2000

High speed data converter techniques

Baiying Yu
Iowa State University

High speed data converter techniques

by

Baiying Yu

A dissertation submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Major: Electrical Engineering(Microelectronics)

Major Professor: Dr. William C. Black, Jr.

Iowa State University

Ames, Iowa

2000

Graduate College
Iowa State University

This is to certify that the Doctoral dissertation of

Baiying Yu

has met the dissertation requirements of Iowa State University

Signature was redacted for privacy.
Committee Member

Signature was redacted for privacy.
Committee Member

Signature was redacted for privacy.
Committee Member

Signature was redacted for privacy.
Committee Member

Signature was redacted for privacy.
Major Professor

Signature was redacted for privacy.
For the Major Program

Signature was redacted for privacy.
For the Graduate College

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 INTRODUCTION

1.1 Motivation

Since digital signals are more immune to noise than analog signals, complex signal processing is usually more straight forward in the digital rather than analog domain. The rapid evolution in digital integrated circuit technologies has led to ever more sophisticated signal processing systems. For these systems to be successful, however, analog-to-digital converters (ADC) and digital-to-analog converters (DAC) are required which translate the real world analog signals into digital signals and vice versa.

In this dissertation, high speed data converter techniques are proposed and demonstrated that lead to high speed and high resolution data converter design. High speed ADCs find extensive applications in digital oscilloscopes, broadband communication and storage devices, such as Hard Disk Drives (HDD). The first part of this dissertation concentrates on high speed techniques for ADCs. The techniques are suitable for Hard Disk Drive applications. High speed and high resolution digital-to-analog converters are necessary for measurement equipment, digital video systems and digital audio applications. The second part of this dissertation concentrates on the techniques for digital-to-analog converters. A

novel and linear Voltage Controlled Resistor (VCR) that is suitable for high speed and high resolution digital-to-analog converter is demonstrated.

1.1.1 High speed analog-to-digital converter techniques

The classic Moore's law graph (Figure 1) shows the increase in maximum possible capability per single IC chip over the three decades since 1960 [1]. Moore's law not only applies to semiconductor technology, it also applies to Hard Disk Drive (HDD) systems over the last 35 years and it will probably continue to do so in the future.

Data storage devices find extensive application in communication, computing and entertainment systems. Storage devices can be divided into several categories depending

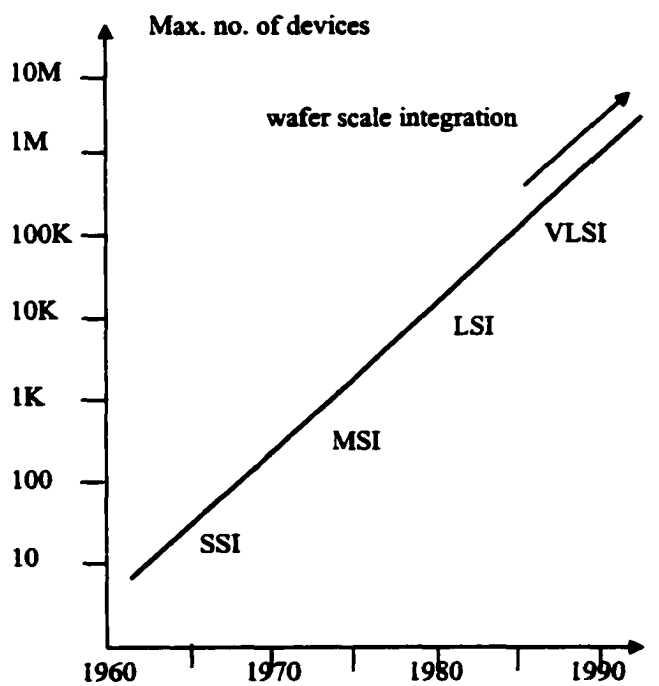


Figure 1 The classic Moore's Law Graph

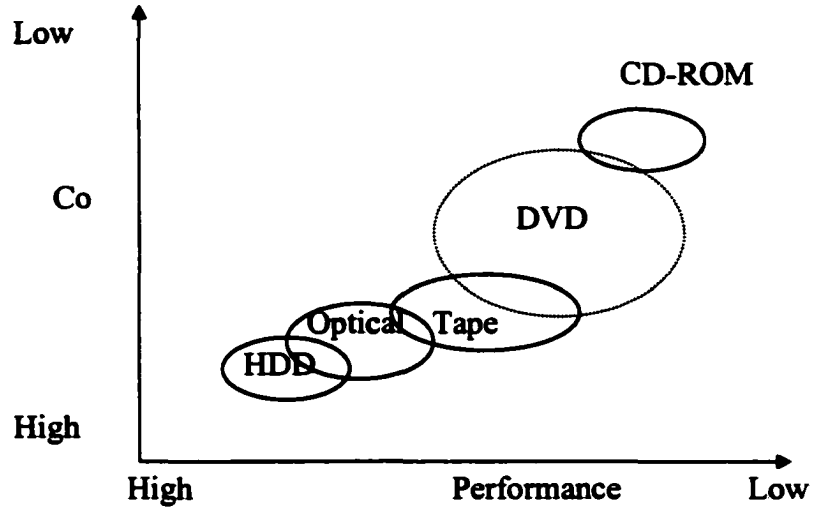


Figure 2 Data Storage devices segmentation

upon the application [2]. Figure 2 shows the relationship between the cost and performance of commonly used storage devices, such as CD-ROM, DVD and HDD, etc.

Because of the low cost of CD-ROM where the access time is on the order of hundreds of milliseconds, it has been used for software and audio distribution. File backup and archival storage rely on low cost and low performance tape systems. For real-time transactional systems where high performance is required, the higher cost system Hard Disk Drive (HDD) which have access time on the order of tens of milliseconds have been used. In order to meet the emerging demands of high performance computing applications, HDD will continue to evolve at a very rapid pace. Advances in read channel technology over the past few years have contributed to the large growth in HDD markets.

Hard disk drives (HDD) currently use Partial- Response Maximum Likelihood (PRML)

signal processing to increase areal density. PRML is a powerful method which can deal effectively with Inter-Symbol Interference (ISI). In most architectures, a high speed ADC is required for the PRML signal processing. The requirement for ADC is follows [2]: 1) 6b resolution; 2) speed as high as possible; 3) More than 5 Effective Number Of Bits (ENOB). In Figure 3, the typical architecture of PRML read channel is shown [3]-[7]. The signal stored on the hard disk drive can be sensed by the magnetic sensor at the front end. Then, the millivolt signal will be amplified by a low noise amplifier VGA. The gain of the VGA will be controlled through the gain control loop. After that, the signal will be filtered to avoid aliasing before the ADC. After the FIR equalizer, it will be detected by the Viterbi circuit. Then, a DSP will process the data. Because of the very high speed operation requirements, most of the ADCs for these circuits are presently implemented using flash architecture [8]-[14].

FLASH architecture provides the highest speed using $2^n - 1$ comparators to perform an n-bit conversion. As shown in Table 1, ten out of the top eleven high speed analog-to-digital converters are flash converters.

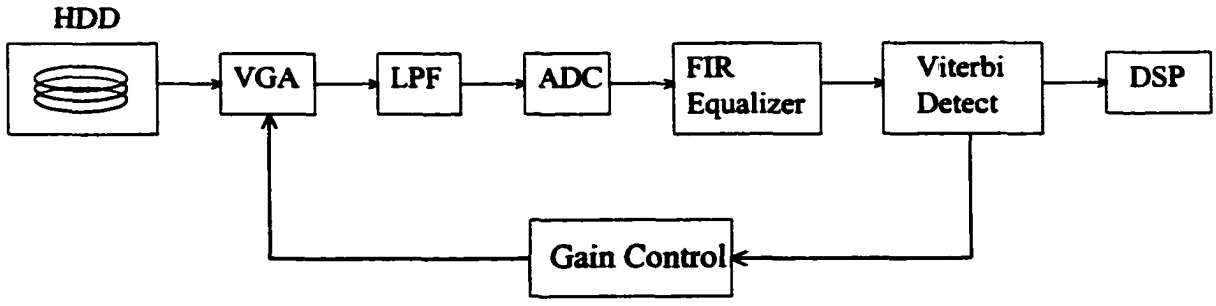


Figure 3 Block diagram of PRML read channel

Table 1 Rank-ordered ADCs by speed figure of merit

Author	Type	Speed	Technology	# of bits	Power (mW)
Xiao [15]	Flash	8G	SiGe	4	500
Ducourant [16]	Flash	3G	GaAs	4	150
Ducourant [17]	Flash	2.2G	GaAs	5	300
Wakimoto [18]	Flash	2G	Bipolar	6	2000
Poulton [19]	Interleaved flash	1G	GaAs	6	16000
Uyttenhove [8]	Flash	1G	0.35um CMOS	6	?
Sushihara [9]	Flash	800M	0.25um CMOS	6	400
Nagaraj [10]	Flash	700M	0.25um CMOS	6	187
Valberg [20]	Folding	650M	Bipolar	8	850
Matsuzawa [21]	Flash	600M	Bipolar	8	4000
Tamka [22]	Flash	500M	0.4um CMOS	6	400

In the extremes of speed, however, exotic technologies must still be used to achieve conversion rates beyond those obtained with a conventional silicon implementation [15]-[17][23]. In this research, a 4-way, time-interleaved flash ADC is demonstrated to achieve conversion speed up to 900MS/s using a 2.5v digital .25 micron bulk CMOS process. The maximum conversion rate practical with any technology is extended by the use of an array of well-matched flash ADCs. This technique trades off increased die area for increased speed in a nearly one for one relationship but at reduced performance if the ADCs are not well matched in terms of gain, offset, nonlinearities and sampling skew [24]. In the approach

considered here, these problems are minimized by use of a simple method that ensures the individual ADC gain, offset and nonlinearity characteristics are inherently almost identical. A simple four phase clock generator is demonstrated which introduces only a small sampling skew. While this scheme has been demonstrated in the comparatively simple 6-bit flash ADC case, this same scheme may be applied to the first n-bits of a pipeline converter (or other converter method) enabling the same identical performance in the most significant bits.

1.1.2 VCR for mismatch adjustment in analog CMOS circuits

High linearity and high resolution A/D and D/A converters are necessary for measurement equipment, digital video systems and digital audio applications. In digital video systems, more complicated and advanced signal processors are needed for digital video processing to enhance video quality. Therefore, high resolution and high speed Digital-to-Analog converters are required to convert digital signal to analog signal. Especially in HDTV and next generation camcorders, high resolution (more than 10 bits) and high speed (faster than 80MHz) D/A converters are needed [25]. High resolution D/A converters are also demanded in digital audio applications, such as Compact Disc Players [26]. Based on matching of components in a standard process only, it is very difficult to achieve such high accuracy. In order to achieve such high resolution, a commonly used method is the Sigma-Delta architecture, which exchanges speed for resolution. So, in order to achieve high speed and high resolution, the analog circuits often require laser trimming or digital error correction of precision components for reasons of linearity or offset adjustment. Therefore, additional calibration techniques are introduced. However, with some calibration techniques, a special

calibration period is required [26]. During this calibration period, the converter can't be used for conversion, which makes this technique limited in some application. Other calibration techniques, like laser trimming and external adjustment increase the cost too. Also, those methods are ofter sensitive to temperature and aging.

A favorable alternative is dynamic element matching [28] which dynamically adjusts components (typically current sources) in order to make them match. When implemented with conventional MOSFETs, however, switch feedthrough [29] effects limit the usefulness of the scheme unless circuitry is made either very large or very slow. This is because precise error adjustment currents on the order of the required mismatch (a few percent for high resolution application) are difficult to realize unless device ratios are made very large or clock transitions are made to be very slow. These drawbacks are eliminated in our scheme which slightly modulates the resistivity of a standard well resistor in order to achieve necessary current matching. This technique can be used to produce multi copies of current units. Therefore, it is suitable for the calibration of high-resolution D/A converters that are based on equal current sources.

1.2 Organization

In chapter 2, both static and dynamic characteristics of ADCs are introduced. DC testing and dynamic testing of ADCs are discussed also. In chapter 3, error sources in flash A/D converters are studied. Timing error is analyzed in detail. In chapter 4, a prototype of time-interleaved A/D converter architecture is proposed. The mismatch between the converters is analyzed in terms of timing skew, gain mismatch and converter offset. Two chips have been

designed with this new architecture and detailed analysis of both architectural considerations and circuit design blocks are discussed. In chapter 5, digital end circuitry of the converter is discussed and simulation results are demonstrated. Layout is a very important issue in the whole procedure and is discussed in chapter 6. In chapter 7, testing setup and testing results are demonstrated. In chapter 8, the properties of the new VCR structure will be studied. The structure and characteristics of the VCR will be analyzed and a new model proposed. In chapter 9, a favorable current calibration principle is introduced. A new calibration principle with VCRs for matched current sources is proposed and simulation of this scheme is demonstrated. A conclusion is given in chapter 10.

CHAPTER 2 CHARACTERIZATION OF ADC

There are a number of ways to measure and evaluate ADC performance. Here we only focus on primarily those characteristics that are important in Hard Disk Drive applications. Static characteristics of ADC include Integral Nonlinearity (INL), Differential Nonlinearity (DNL), gain error and missing codes. The dynamic characteristics of A/D converters are usually signal to noise ratio (SNR), SNDR, ENOB and SFDR. In this chapter, the characterizations of ADC are discussed.

2.1 Static characteristics

Integral nonlinearity is the deviation from a characteristic line. The characteristic line can be defined differently. It can be the line connecting the endpoints of the converter's transfer curve. Or, it can be defined as the best fit line of the converter's transfer curve.

Assuming the linear function for the characteristic line is

$$y = ax + b \qquad (1)$$

And the function for the real transfer curve of ADCs is

$$y = f(x) \qquad (2)$$

Then, the integral nonlinearity (INL) can be derived using equation (3) .

$$INL(x) = f(x) - (ax + b) \qquad (3)$$

In Figure 4, integral nonlinearity error in a 3-bit A/D converter is shown, along with differential nonlinearity (DNL) and missing code. In an ideal data converter, each analog step is 1LSB. Differential nonlinearity (DNL) defines the deviation of the analog step from 1LSB

Assuming each digital output code y_i corresponds to a range of analog inputs between x_{i-1} and x_i. Then, the differential nonlinearity (DNL) can be derived.

$$DNL_i = x_i - x_{i-1} - 1LSB \qquad (4)$$

The nonlinearity of the converter is usually summarized as the maximum absolute DNL and INL. If the maximum of DNL of an ADC is greater than 1LSB, missing code will appear in its transfer curve. Both DNL and missing codes are demonstrated in Figure 4 also[30].

Gain error is the deviation of the real characteristic line from the ideal characteristic line. A small constant gain error or offset usually is not a big concern in most applications.

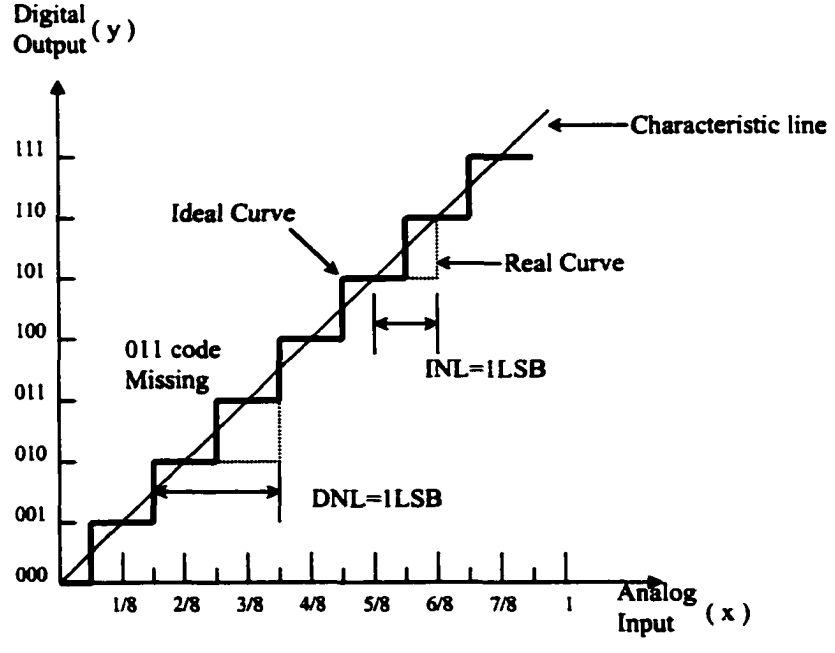


Figure 4 Transfer curve of 3b A/D Converter

2.2 DC testing of analog-to-digital converter

Figure 5 shows the testing setup for static performance of an ADC. Usually, the D/A used here should have relatively higher performance than the analog-to-digital converter under test. A slow linear ramp signal generated by the signal source feeds into the ADC. Then, the digital output will be translated into an analog signal by the DAC. The output of the DAC is subtracted from the input signal. By doing this, INL and DNL of the ADC can be measured.

An alternative way of measuring the linearity of an ADC is Code Density Test (CDT), which evaluates the histogram of the generated output codes [31][32]. The main advantage of Code Density Test (CDT) is that it allows us to test the ADC without the need for a high speed high resolution DAC which is required in a traditional measurement technique, as shown in Figure 5. The output of code density or histogram is the number of times each individual code occurs. For example, with a full scale ramp and an ideal ADC, the possibility for each individual code is the same. In this case, the histogram should be uniformly

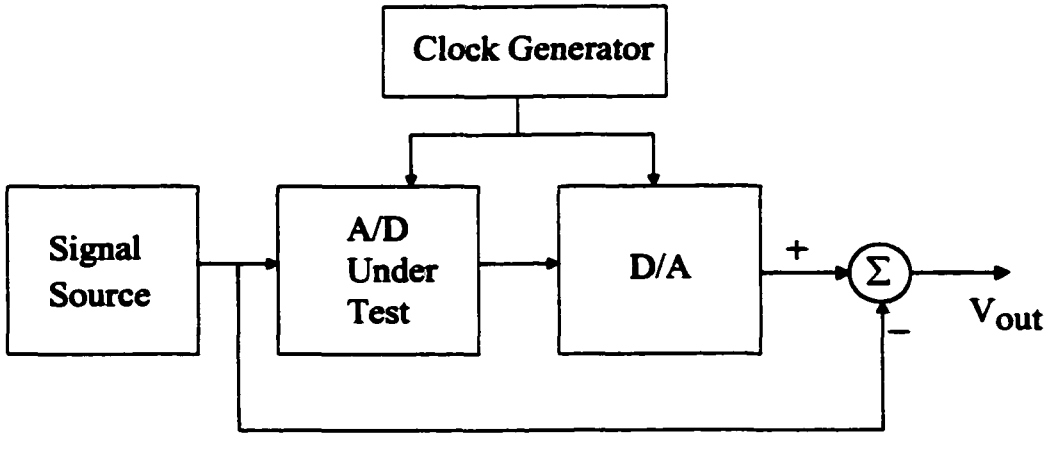


Figure 5 Testing of static characteristics

distributed. Any output code density equal to zero indicates a missing code. The result of the Code Density Test (CDT) gives the direct result of differential nonlinearity (DNL). By integration of the measurement results, integral nonlinearity (INL) can be derived. The choice of the input waveform can also be a pure sine wave since the mathematical model of the pure sine wave is well known to us. However, the nonlinearity estimated by CDT does not provide precise information on the performance of high resolution ADCs [33].

2.3 Dynamic characteristics

As we mentioned before, analog-to-digital converters translate the analog signals into digital signals. All analog-to-digital converters have finite resolution. During analog-to-digital conversion, quantization error is introduced due to finite resolution.

In Figure 6, the residue after conversion is plotted (assuming the input signal is a slow linear ramp). The residue is defined as follows.

$$residue = y(LSB) - x(LSB) \qquad (5)$$

This residue is so called quantization error. As we can see, for an ideal A/D converter, the

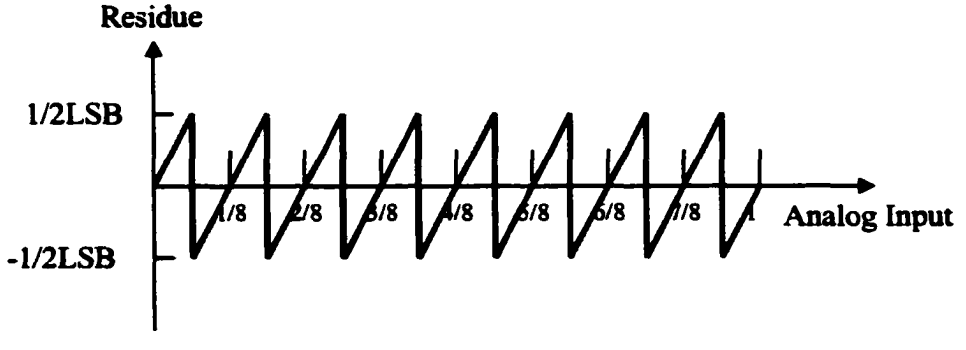


Figure 6 Residue of a 3-bit A/D Converter

quantization error is in the range of (-1/2LSB, 1/2LSB). Then the mean-square-error due to quantization can be calculated.

Assuming the quantization error is uniformly distributed in the range of (-1/2LSB, 1/2LSB), the rms of quantization error can be represented by:

$$V_n^2 = \frac{1}{12} LSB^2 \qquad (6)$$

Assume Vpp is the peak-to-peak voltage of the input sine wave. The rms value of the input sine wave is represented by

$$V_s^2 = \frac{1}{2} V_{pp}^2 \qquad (7)$$

where Vpp is equal to 2^{n-1}LSB.

Assuming the quantization error of a sine wave is the same as in equation (6). Then, the signal to noise ratio for a sine wave input can be calculated as follows.

$$S/N = \frac{V_s}{V_n} = \frac{2^{n-1} LSB}{\sqrt{2}\frac{1}{12} LSB} = \sqrt{1.5}2^n \qquad (8)$$

The signal to noise ratio can be expressed as (9) also.

$$S/N = 6.02n + 1.76 \ (dB) \qquad (9)$$

Equation (9) is derived by assuming uniformly distributed quantization error for a sine wave input. However, it is intuitively known this is not true [34]. For a sinusoidal signal, the probability density function (PDF) of x is given by

$$f_x(x) = \frac{1}{\pi\sqrt{A^2 - x^2}} \qquad (10)$$

where x is regarded by the quantizer as a random variable and A is a multiple of the quantizing step. The quantization error (normalized with respect to quantizing step) can be represented by [34]

$$V_n^2 = \frac{1}{12} + \frac{1}{\pi^2} \sum_{n=1}^{\infty} \frac{(-1)^n}{n^2} J_0(2\pi nA) \qquad (11)$$

$J_0(2\pi nA)$ is a Bessel function of zeroth order. As A increases, the quantization error approaches to a normalized value of 1/12, which is the same as shown in equation (6).

Due to the nonlinearity of the circuitry, harmonic distortion can be introduced. SNDR is defined as the ratio of the signal power to the total of noise power and harmonics power. ENOB is defined based on SNDR. The definition of ENOB is shown in equation (12).

$$ENOB = (SNDR - 1.76)/6.02 \qquad (12)$$

With equation (12), if Signal to Noise and Distortion Ratio (SNDR) is known, then Effective Number Of Bits (ENOB) can be calculated.

Another important characteristic of ADC is the Spurious Free Dynamic Range (SFDR). SFDR is defined as the ratio between the fundamental signal and the largest distortion component.

2.4 Dynamic testing of analog-to-digital converter

Figure 7 shows the setup for the dynamic performance of ADC. The input sine wave signal generated from the signal source will go through a low pass filter to remove the harmonic distortion. The digital output from the ADC will be captured by the high speed logic analyzer and translated into analog signal. Then, the signal can be analyzed by using a

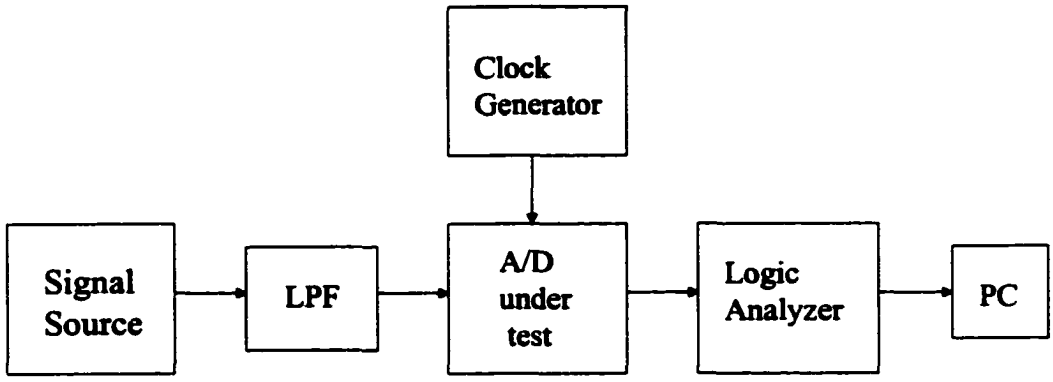


Figure 7 Dynamic testing setup for ADC

Fast Fourier Transform (FFT). Enough samples are needed to obtain accurate information. In order to minimize the "leakage" due to FFT, a window function must applied. With the frequency information from FFT, SNR, SNDR and ENOB can be calculated. ENOB can be determined via histogram testing also [39].

CHAPTER 3 ERROR SOURCES IN FLASH A/D CONVERTER

3.1 Generic scheme of flash A/D Converter

In Figure 8, a generic scheme of flash A/D converter is shown. Comparators of $2^n - 1$ are used to locate the position of the analog input relative to the reference voltage which usually are generated from the resistor string.

All the comparators will sample its corresponding reference voltage first, then, the

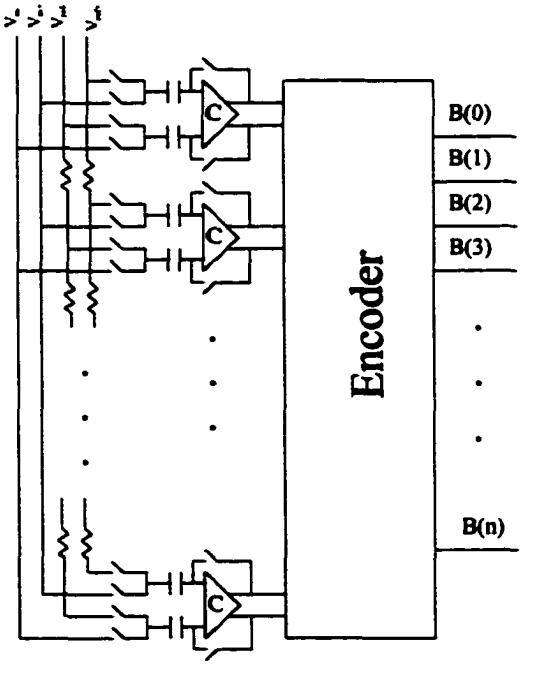


Figure 8 Generic scheme of flash ADC

sampling capacitors are switched to the analog input. Each comparator will compare the differential analog signal with its differential reference voltage sampled and send out the digital signal as '0' or '1' simultaneously. If the analog signal is greater than the reference voltage, the digital output of the comparator is '1'. Otherwise, it is '0'. The combined output of all the comparators appears as thermometer code, ones at the bottom while zeros at the top. The transition from '1' to '0' depends upon the analog voltage level. Ideally, there is only one transition point where the digital code changes from '1' to '0'. Then, the transition will be detected and the output 'high' will be translated into binary code by an encoder. There are many things that could possibly go wrong. In the following sections, the error sources of this scheme will be analyzed in detail.

3.2 Comparator offset

In a flash A/D converter, comparators make decisions between the analog input V_{in} and its reference voltage V_{ref}. When V_{in} is greater than V_{ref}, it sends out digital signal '1'. When Vin is less than V_{ref}, the digital output is '0'. However, this is how the ideal comparator works. In reality, each comparator has its own offset. In Figure 9, the comparator offset is shown at the input as V_{os}. In this case, instead of comparing V_{in} to V_{ref}, the comparator is making decision between $V_{in} \pm V_{os}$ and V_{ref}.

Comparator offset may be contributed by several sources. One comes from the process mismatch, which contribute static offset to the comparator. There are many offset reduction techniques to compensate the offset [35]. A simple technique to reduce the static offset is by

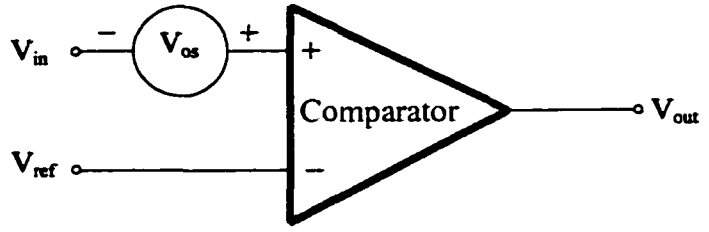


Figure 9 Comparator offset

doing auto-zeroing [38]. Another contribution is the charge injection during switching, which is dynamic offset of the comparator caused by switches. Proper switch phasings can to some degree minimize the dynamic offset.

Because of the comparator offset, the combined output of the comparators may not remain as a thermometer code any more, especially at high speed. It may have a "bubble" in it, just like bubbles in thermometer. In other words, the transition from '1' to '0' does not happen only once, it may happen several times. Simply detecting the transition from '1' to '0' based on a simple two input NAND gate or NOR gate may cause dramatic errors in encoding. Several techniques have been employed in this design to minimize encoding error.

3.3 Timing error without sample and hold

Another important error source is timing error. In an ideal flash ADC, all the comparators compare the same analog input with different reference levels. This requires the same propagation delay of both clock signal and analog signal traveling for 2^n-1 comparators. In reality, this is impossible. If we can have a sample and hold at the input of the analog signal, the effect of timing skews can be minimized. In this section, we will explore the possibility of having a sample and hold for the analog input signal.

3.3.1 Operational Amplifier

Let's find out in order to achieve 6b accuracy at sampling rate 600Msample/s, what the bandwidth of the operational amplifier needs to be [43]? Figure 10 shows the block diagram of an Opamp in its hold phase.

Assume the transfer function of the operational amplifier is as follows,

$$A(s) = \frac{A_0}{1 + s\tau} \qquad (13)$$

where A_0 is the DC gain of the operational amplifier, τ is the time constant of the open loop.

The close loop gain G is defined as

$$G = \frac{V_o}{V_i} = -\frac{\frac{A_0}{A_0 + 2}}{1 + s\tau_{FB}} \qquad (14)$$

where τ_{FB} is the time constant of the closed loop.

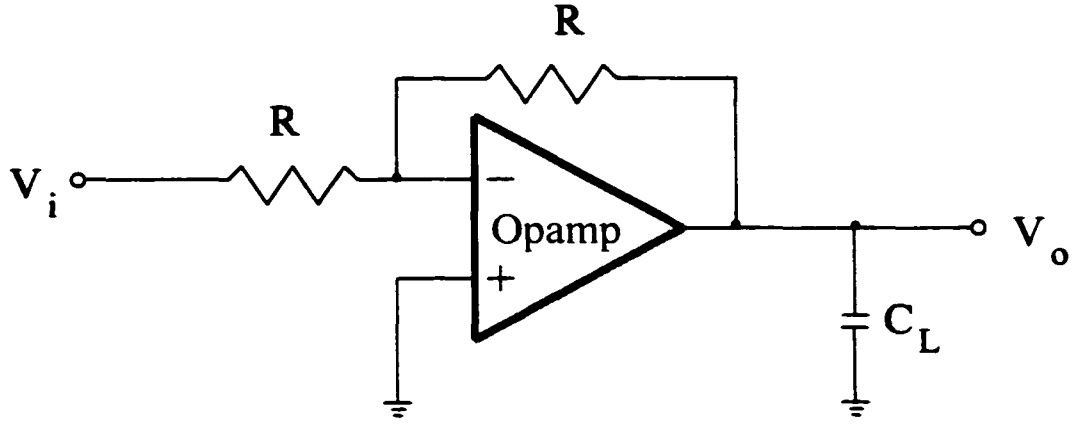


Figure 10 Block diagram of an operational amplifier in its hold phase

If V_i is a unit step and the output of the amplifier is always a linear function of its input, the output would be

$$V_0(t) = -\frac{A_0}{A_0 + 2}[1 - e^{\frac{-t}{\tau_{FB}}}] \qquad (15)$$

For the output to settle within 1/2LSB at its final value, the following condition needs to be met,

$$V_{ref}[1 - e^{\frac{-t}{\tau_{FB}}}] \geq V_{ref}[1 - \frac{2}{2^{n+1}}] \qquad (16)$$

The condition can be rewritten as:

$$t \geq n\tau_{FB} \ln(2) \qquad (17)$$

For an operational amplifier to get 6 bits resolution with sampling frequency at speed 600Msample/s, the 3dB bandwidth of the closed loop needs to be greater than 2.5GHz. Due to relatively high capacitive load of C_L, it is practically impossible to achieve this high speed Opamp using most advanced CMOS technology.

3.3.2 Source follower

An alternative way to achieve a sample and hold is using a simple source follower as shown in Figure 11 along with sampling switch S_1. However, switch induced error, error due to input dependent sampling instant and most of all, error induced due to nonlinearity of the source follower will distort the analog signal. All these error sources related with the source follower as a sample and hold are analyzed in detail in this section.

3.3.2.1 Switched induced error

The error voltage induced by the turning off of the switch is one limiting factor in the scheme shown in Figure 11 [44]. When the switch S_1 turns off, some portion of the charges in the channel of the switch transistor is transferred to the gate of M_1 and causes error. As we can see, the error is input dependent. Even though fully differential scheme will minimize the error, however, it can not be canceled exactly. For slow switching-off,

$$\frac{\beta V_{HT}^2}{2C_L} >> U$$

The error induced on the sampling capacitor C_L

$$v_e = \left(\frac{C_{ol} + \frac{C_{ox}}{2}}{C_L}\right)\sqrt{\frac{\pi U C_L}{2\beta}} + \frac{C_{ol}}{C_L}(V_s + V_T - V_L) \qquad (18)$$

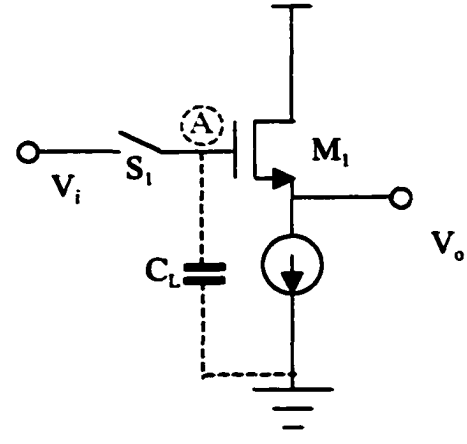


Figure 11 Source follower as sample and hold

where

$$\beta = \mu C_{ox} \frac{W}{L} \quad and \; V_{HT} = V_H - V_s - V_T$$

V_H and V_L are high and low voltage level for clock signal. V_S is the source voltage of the switch, which is equivalent to V_i in Figure 11. U is the slope of the falling edge of the clock. C_{ol} is the overlap capacitance of the switch transitor and C_{ox} is the gate capacitance of the switch transistor. For fast switching-off,

$$\frac{\beta V_{HT}^2}{2C_L} << U$$

$$v_e = \left[\frac{C_{ol} + \frac{C_{ox}}{2}}{C_L} \right] \left[V_{HT} - \frac{\beta V_{HT}^3}{6UC_L} \right] + \frac{C_{ol}}{C_L}(V_s + V_T - V_L) \qquad (19)$$

For a fully differential scheme, the switch induced error would be

$$V_{diff} = \frac{C_{ol}}{C_L}(V_{S1} - V_{S2}) \qquad (20)$$

Assume the overlap capacitance C_{ol} is 1% of C_L, and V_{S1}-V_{S2} is 2 volt, then the switch induced error would be 20 millivolts. From equation (20), we can easily observe that the smaller the C_{ol}/C_L, the smaller the error. However, small C_{ol}/C_L conflicts with high speed operation requirements. Besides, the switch induced error tends to be bigger due to mismatch of the input pairs in fully differential structure.

3.3.2.2 Input dependent sampling error

The NMOS switch will only be turned on when the gate voltage is higher than the input by V_t. If the analog input is not constant, the real sample points differ depending on the analog

input. As we can see in Figure 12, the real sampling time is different from the ideal sampling time and the sampling instant depends on the input signal. Based on this fact, it has been shown that harmonic distortion will be introduced[45].

Signal to Distortion Ratio (SDR) can be predicted using equation (21).

$$SDR_{\max} = 20\log 10(\frac{V_{CK}}{Af_{in}t_F}) \qquad (21)$$

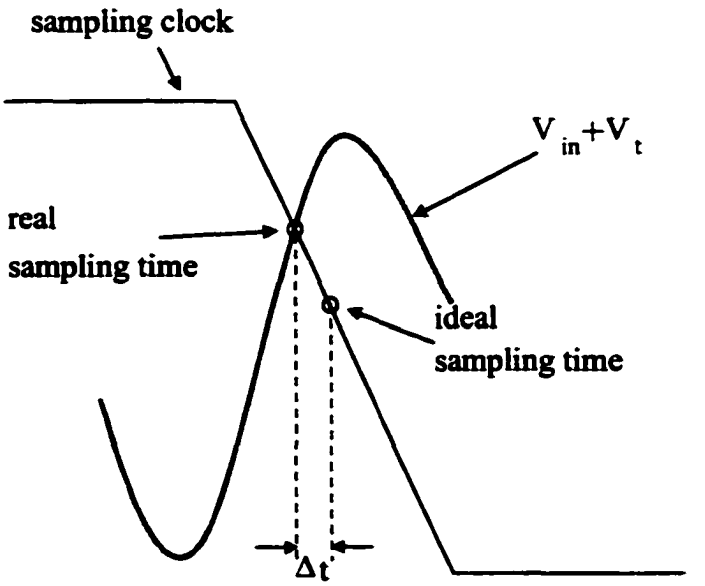


Figure 12 Input dependent sampling skew

where V_{CK} is the voltage swing of the clock, f_{in} is the frequency of the input signal and t_F is the falling time of the sampling clock Assume the voltage swing of the sampling clock is 2.5 volts, the amplitude of the analog input signal is 500mv, the frequency of the analog input signal is 250MHz, and the clock falling time is 200ps, then the maximum signal to distortion ratio SDR_{max} is 40dB. Bootstrap schemes may minimize the error, however, they limit the speed [36][37].

3.3.2.3 Nonlinearity of source follower

Another common problem with a simple source follower is the nonlinearity of its transfer curve over a wide range. Two sources contribute to its error. First of all, is the length modulation effect that makes the output impedance of the transistor a finite value. The second source is the back bias that modulates the threshold voltage of the transistor. By connecting the substrate of M_1 to its source, it will improve the linearity of the source follower [47]. Because of all the error sources discussed above, it is very difficult to design a source follower which has more than 6 bits accuracy for 250MHz analog input with 2.5 volts power supply.

Without a sample-and-hold at the analog input, each comparator may sample the analog input at different times due to different propagation delays for each signal path. Figure 13 shows the relation between the Effective Number of Bits (ENOB) and timing jitter simulated using Matlab by averaging 100 converters with the assumption that the timing jitter is normally distributed with zero mean. As we can see, around 20ps timing error will introduce

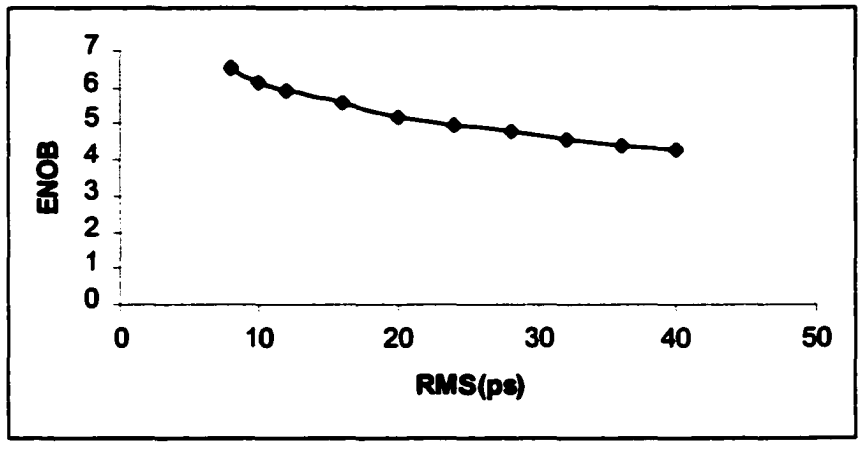


Figure 13 The relation between ENOB and timing jitter

about 1bit error into 6b ADC system at Nyquist rate when sampling at a speed of 500Msample/s. This places a very strict requirement both for clock generation and clock distribution.

3.4 Gain error

As we discussed before, the comparator array compares the input signal with the reference and generates the corresponding digital output. At full scale, The peak-to-peak voltage of the input signal should be the same as the reference voltage. But what if the reference voltage is less than the V_{pp} of the analog input? From the simulation using Matlab, we can see that the output spectrum will have the odd harmonic components of the analog input. In Figure 14, the spectrum is shown with gain error.

Using Matlab, we can find out quantitatively how this will affect ENOB due to mismatch

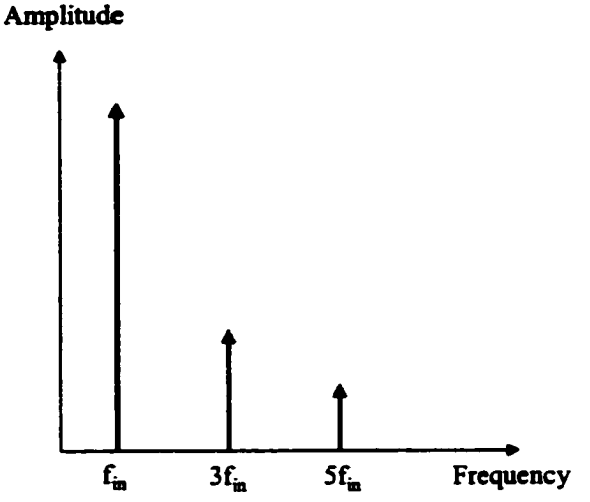


Figure 14 Output spectrum with gain error due to clipping

between the analog input range and reference range. Figure 15 shows the ENOB with the difference between the reference range and analog range normalized in LSB. As we can see, if the reference range is 4LSB less than the analog input range, it will introduce 1bit error into the system.

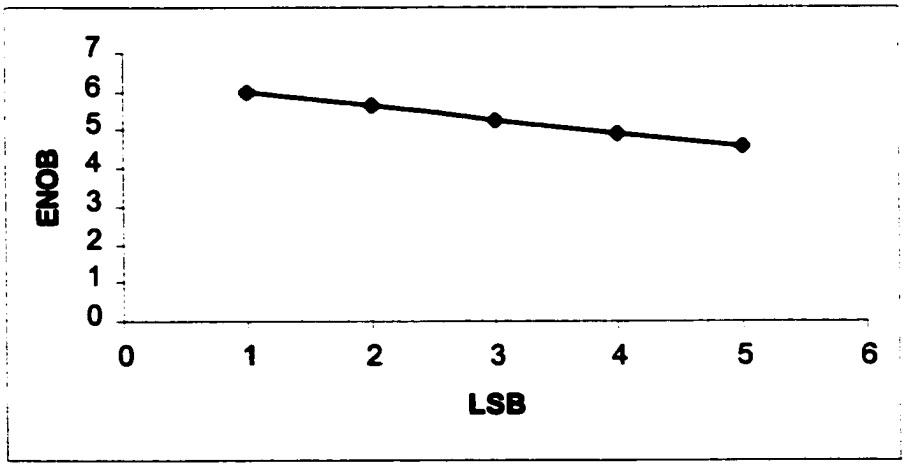


Figure 15 The relation of ENOB with the error between the reference range and the analog input range

CHAPTER 4 PROTOTYPE OF TIME-INTERLEAVED FLASH ADC

High-speed data conversion and signal processing circuits are demanded for data communication, data storage, etc. In the extremes of speed, exotic technologies must be used to achieve data rates beyond those obtained with a conventional silicon implementation [15][16][17]. By using a time-interleaved architecture, the maximum conversion rate practical with any technology is extended by the use of an array of identical channels. This topology applied to an analog-to-digital converter is shown in Figure 16. The timing strategy

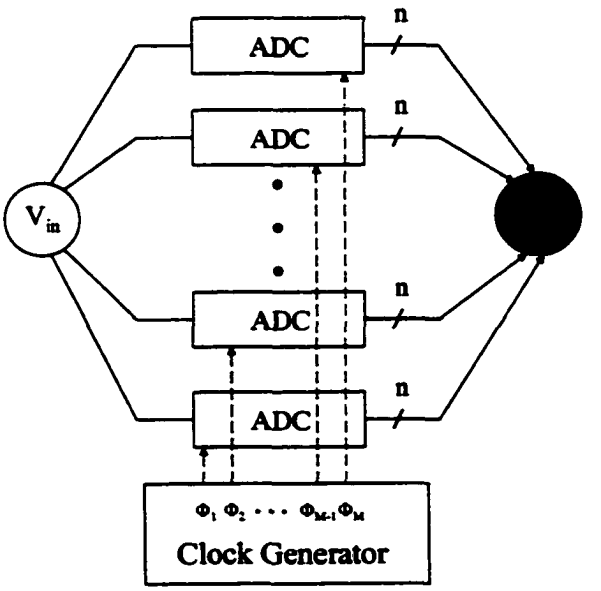


Figure 16 Generic scheme of time-interleaved ADC architecture

of a four-way, time-interleaved ADC is shown in Figure 17. Basically, each individual ADC is running at a speed of 1/T but at different clock phases that are generated by the multi-phase clock generator. Ideally, the phase differences between adjacent clocks are the same. The outputs from four converters can be combined by a high speed 'MUX', resulting in a high

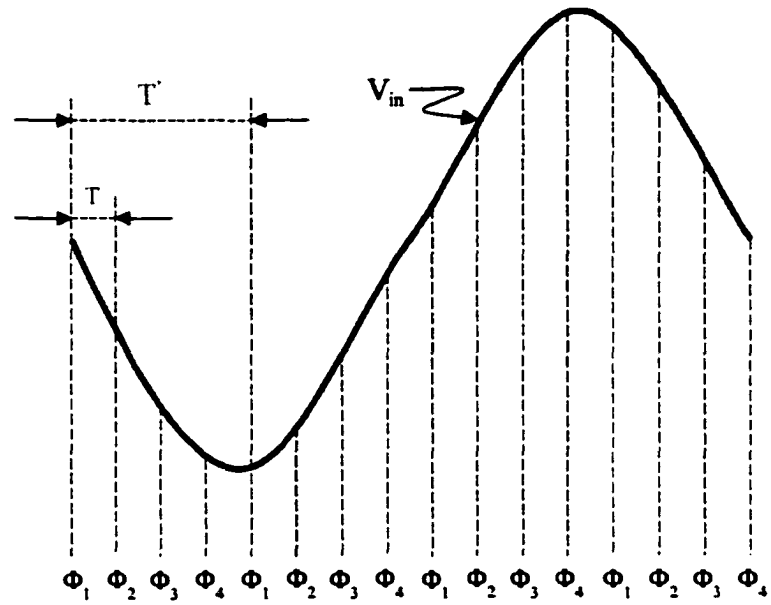


Figure 17 Timing of ADC

speed ADC with a sampling speed of 4/T. So, the sampling frequency of the whole ADC is extended by four times. By doing this, the speed requirements for each sub-ADCs are relaxed.

All the error sources mentioned before will also introduce errors into time-interleaved flash A/D converter. Besides those error sources mentioned in the previous chapter, the mismatch between the converters offset and gain will also degrade the performance of the ADC, as does the phase skew between the channels. Before we get into the design detail of

the prototype of four-way, time-interleaved flash analog-to-digital converter, the error due to mismatch between channels will be analyzed.

4.1 Error analysis in time-interleaved analog channels

As we discussed earlier, time-interleaved techniques trade off increased die area for increased speed in a nearly one for one relationship but at reduced performance if the analog channels are not well matched in terms of gain, offset and sampling skew.

4.1.1 Phase skew

As we discussed before, a high speed operational amplifier is very difficult to design for use in a sample-and-hold. If we eliminate the sample and hold at the analog input, however, timing differences with the analog channels will degrade performance, usually called phase skew.

For an m-way converter array, assume the original sampled data sequence is [48]

$$S = [f(t_0), f(t_1), f(t_2), \ldots, f(t_M), f(t_{M+1}), \ldots] \qquad (22)$$

The digital spectrum, F(ω), of S can be represented by

$$F(\omega) = \frac{1}{MT} \sum_{m=0}^{M-1} \left[\sum_{k=-\infty}^{\infty} F^a \left[\omega - k\left(\frac{2\pi}{MT}\right) \right] e^{j[\omega - k(2\pi/MT)]t_m} \right] e^{-jm\omega T} \qquad (23)$$

Assume the systematic timing error for each channel is $r_m T$, then

$$t_m = mt - r_m T \qquad (24)$$

T is the sampling period of the composite array.

For a sinusoidal $e^{j\omega_{in}t}$, the Fourier transform is given by

$$F^a(\omega) = 2\pi\delta(\omega - \omega_{in}) \qquad (25)$$

Substituting (25) into (23), we have

$$F(\omega) = \frac{1}{MT}\sum_{m=0}^{M-1}\sum_{k=-\infty}^{\infty} 2\pi\delta[\omega - \omega_{in} - k(2\pi/MT)]e^{-jr_m 2\pi f_0/f_s}e^{-jkm(2\pi/M)} \qquad (26)$$

where f_s is the sampling frequency, which is equal to 1/T. f_0 is equal to $2\pi/\omega_0$.

Equation (26) can be rewritten as

$$F(\omega) = \frac{1}{T}\sum_{k=-\infty}^{\infty} A(k)2\pi\delta\left[\omega - \omega_{in} - k(\frac{2\pi}{MT})\right] \qquad (27)$$

where

$$A(k) = \sum_{m=0}^{M-1}\left[\frac{1}{M}e^{-jr_m 2\pi f_{in}/f_s}\right]e^{-jkm(2\pi/M)} \qquad (28)$$

For a sine wave input, the Fourier transform is given by

$$F^a(\omega) = j\pi[\delta(\omega + \omega_{in}) - \delta(\omega - \omega_{in})] \qquad (29)$$

Substitute (29) into (23), we have

$$F(\omega) = \frac{1}{T}\sum_{k=-\infty}^{\infty}[A(k)2\pi\delta(\omega + \omega_{in} - k\frac{2\pi}{MT}) + B(k)2\pi\delta(\omega - \omega_{in} - k\frac{2\pi}{MT})] \qquad (30)$$

where

$$A(k) = \frac{-1}{2j}\sum_{m=0}^{M-1}[\frac{1}{M}e^{jr_m 2\pi f_{in}/f_s}]e^{-jkm(2\pi/M)} \qquad (31)$$

$$B(k) = \frac{1}{2j}\sum_{m=0}^{M-1}[\frac{1}{M}e^{-jr_m 2\pi f_{in}/f_s}]e^{-jkm(2\pi/M)} \qquad (32)$$

It is very easily to prove that

$$A(k) = -B^*(M-k) \qquad (33)$$

From equation (30), we can observe that due to timing skew, the digital spectrum comprises M pairs of line spectra, each pair centered at the fractional of the sampling frequency of f_s, such as $f_s/M, 2f_s/M, ..., (M-1)f_s/M$. Table 2 summarizes the digital spectrum in the frequency range of $(0, f_s)$ for a four-way, time-interleaved array.

Table 2 Summary of the digital spectrum with timing skew

k	Frequency (ω)	Amplitude
0	f_0	| B(0) |
1	$-f_0+f_s/4$	| A(1) | = | B(3) |
	$f_0+f_s/4$	| B(1) |
2	$-f_0+f_s/2$	| A(2) | = | B(2) |
	$f_0+f_s/2$	| B(2) |
3	$-f_0+3f_s/4$	| A(3) | = | B(1) |
	$f_0+3f_s/4$	| B(3) |
4	$-f_0+f_s$	| A(4) | = | B(0) |

The digital spectrum with timing skew for a four-way, time-interleaved array is shown in Figure 18, along with the amplitude for each spectral line. As we can see, due to the timing skew between the channels, the digital spectrum comprises side lobes around the fractions of the sampling frequency. From (31) and (32), we can also observe that the amplitude for each

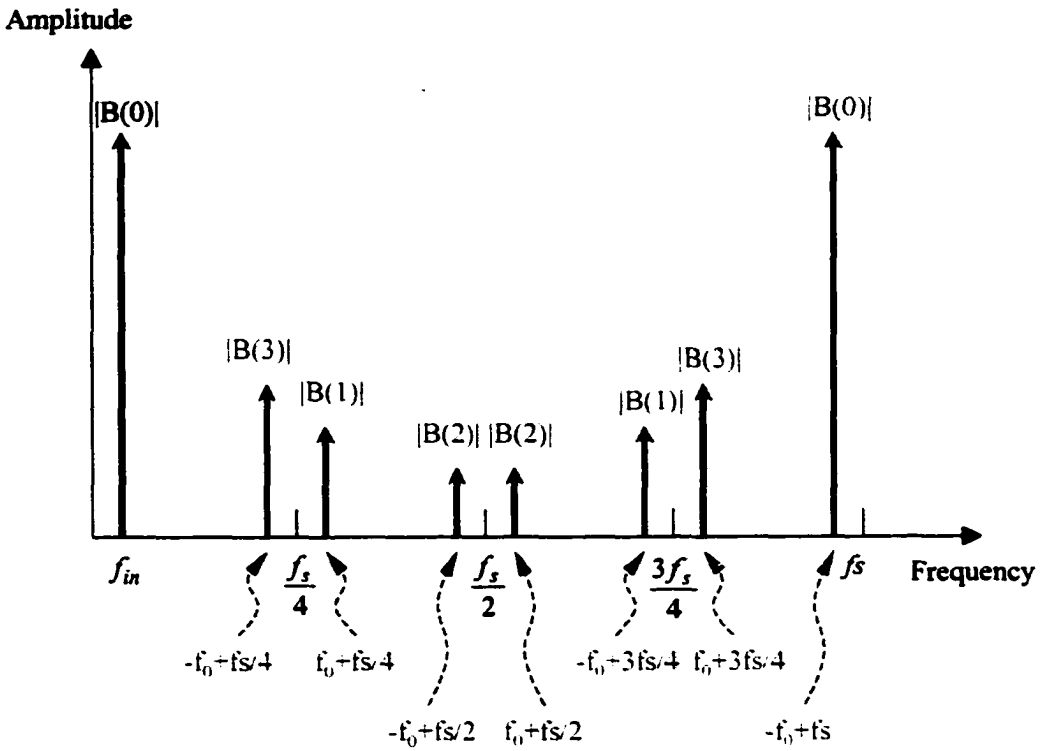


Figure 18 Digital spectrum with timing skew

pair centered at the fractional of the sampling frequency are functions of timing skews which are not necessarily equal to each other.

By Parseval's theorem, we have

$$P_1 = \sum_{k=0}^{M-1} |A(k)|^2 = \frac{1}{4} \qquad (34)$$

$$P_2 = \sum_{k=0}^{M-1} |B(k)|^2 = \frac{1}{4} \qquad (35)$$

The total signal and distortion power is

$$P = P_1 + P_2 = 1/2 \qquad (36)$$

Assume r_m is normally distributed with standard deviation of σ_t and zero mean. The signal power located at ω_0 is

$$
\begin{aligned}
|B(0)|^2 &= \left| \sum_{m=0}^{M-1} \frac{1}{2Mj} e^{-jr_m 2\pi f_{in}/f_s} \right|^2 \\
&= \frac{1}{4} \left| \sum_{m=0}^{M-1} \frac{1}{M} (1 + jr_m 2\pi f_{in} f_s - \frac{1}{2}(r_m 2\pi f_{in}/f_s)^2 \right|^2 \\
&= \frac{1}{4} \left| \frac{1}{M} \sum_{m=0}^{M-1} 1 + j2\pi f_{in}/f_s \frac{\sum_{m=0}^{M-1} r_m}{M} - \frac{1}{2}(2\pi f_{in}/f_s)^2 \frac{\sum_{m=0}^{M-1} r_m^2}{M} \right|^2 \\
&= \frac{1}{4} |1 - \frac{1}{2}(2\pi f_{in}/f_s)^2 \sigma_t^2|^2
\end{aligned}
\tag{37}
$$

The noise power in the range of $(0,1/(2f_s))$ should be

$$
\begin{aligned}
noise &= (P - 2|B(0)|^2)/2 \\
&= \left(\frac{1}{2} - \frac{1}{2} \left(1 - \frac{1}{2}(2\pi\sigma_t f_{in}/f_s)^2 \right)^2 \right)/2 \\
&= \frac{1}{4} - \frac{1}{4} \left(1 - \frac{1}{2}(2\pi\sigma_t f_{in}/f_s)^2 \right)^2
\end{aligned}
\tag{38}
$$

The signal to noise ratio can be obtained

$$
\begin{aligned}
SNR &= 10\log 10 \left(\frac{|B(0)|^2}{noise} \right) \approx 10\log 10 \left(\frac{\frac{1}{4}}{\frac{1}{4} - \frac{1}{4}(1 - \frac{1}{2}(2\pi\sigma_t f_{in}/f_s)^2)^2} \right) \\
&\approx \left(20\log 10 \frac{1}{2\pi\sigma_t f_{in}/f_s} \right)(dB)
\end{aligned}
\tag{39}
$$

From equation (39), we can easily observe that the signal-to-noise ratio (SNR) is a function of $\sigma_t f_{in} / f_s$, where σ_t is the standard deviation of the timing skew, f_{in} is the analog input frequency and f_s is the sampling frequency. If $\sigma_t f_{in} / f_s$ doubles, the signal-to-noise ratio (SNR) will decrease about 6dB.

Figure 19 shows the comparison between the numeric results obtained using equation (39) and the discrete time simulation results. The simulated results were obtained by averaging 100 arrays using Matlab. As we can see, the higher the time-interleaved number M, the smaller the error between the numeric results and the simulated results. If the interleave number is greater than 12, equation (39) can be used to estimate the signal-to-noise ratio very precisely.

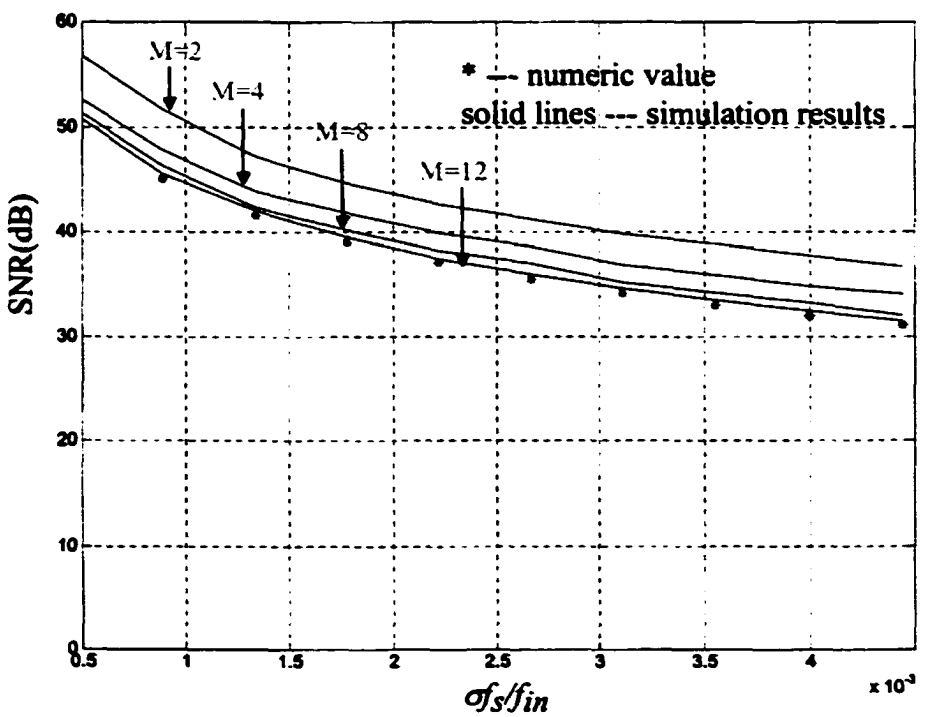


Figure 19 The relationship between SNR and the timing skew

For a four-way, time-interleaved array, the signal-to-noise ratio can be estimated using the equation (40). In order to achieve 6b accuracy at Nyquist rate with sampling frequency of 500MS/s, the timing skew between the different channels needs to be smaller than 12ps based on equation (40).

$$SNR = 20\log 10\left(\frac{1}{2\pi\sigma f_{in}/f_s}\right) + 3(dB) \qquad (40)$$

4.1.2 Gain mismatch

Based on equation (23), we can derive the digital spectrum of time-interleaved arrays with gain mismatch. Gain mismatch can be modeled by making the amplitude of the input signals sampled be different for different channels. Assume for each individual analog channel, the analog input signal is $A_m \sin(\omega_{in} t)$, where m=0, ... M-1. Based on equation (3), we can derive the digital spectrum of the composite time-interleaved array with gain mismatch.

For a sine wave $A_m \sin(\omega_{in} t)$, the Fourier transform is given by

$$F_m{}^a(\omega) = j\pi A_m[\delta(\omega + \omega_{in}) - \delta(\omega - \omega_{in})] \qquad (41)$$

where m=0, 1, ... M-1

Assume there is no timing error, which implies that r_m is equal to zero.

Substituting (41) into (23), we can get

$$F(\omega) = \frac{1}{T}\sum_{k=-\infty}^{\infty} A(k)[2\pi\delta(\omega + \omega_{in} - k\frac{2\pi}{MT}) - 2\pi\delta(\omega - \omega_{in} - k\frac{2\pi}{MT})] \qquad (42)$$

where

$$A(k) = \frac{j}{2M} \sum_{m=0}^{M-1} A_m e^{-jkm\frac{2\pi}{M}} \qquad (43)$$

Table 3 gives the summary of the digital spectrum for a four-way, time interleaved array with gain mismatch. The digital spectrum of the four-way, time-interleaved array is shown in Figure 20. Comparing Figure 20 with Figure 18 which shows the digital spectrum of a four-way, time-interleaved array with timing skew, we can see that both spectra lines are located at the same frequency. The digital spectrum with gain mismatch also comprises M pairs of line spectra that are centered at fractions of the sampling frequency f_s, such as f_s/M, $2f_s/M$, ..., $(M-1)f_s/M$, which is the same as that with timing skew. However, for the digital spectrum with gain mismatch, the amplitude for each pair is the same, which is not necessary true for the digital spectrum with timing skew.

Table 3 Summary of digital spectrum with gain mismatch

k	Frequency (ω)	Amplitude
0	f_0	$\|A(0)\|$
1	$-f_0+f_s/4$	$\|A(1)\|$
	$f_0+f_s/4$	$\|A(1)\|$
2	$-f_0+f_s/2$	$\|A(2)\|$
	$f_0+f_s/2$	$\|A(2)\|$
3	$-f_0+3f_s/4$	$\|A(3)\|$
	$f_0+3f_s/4$	$\|A(3)\|$
4	$-f_0+f_s$	$\|A(4)\| = \|A(0)$

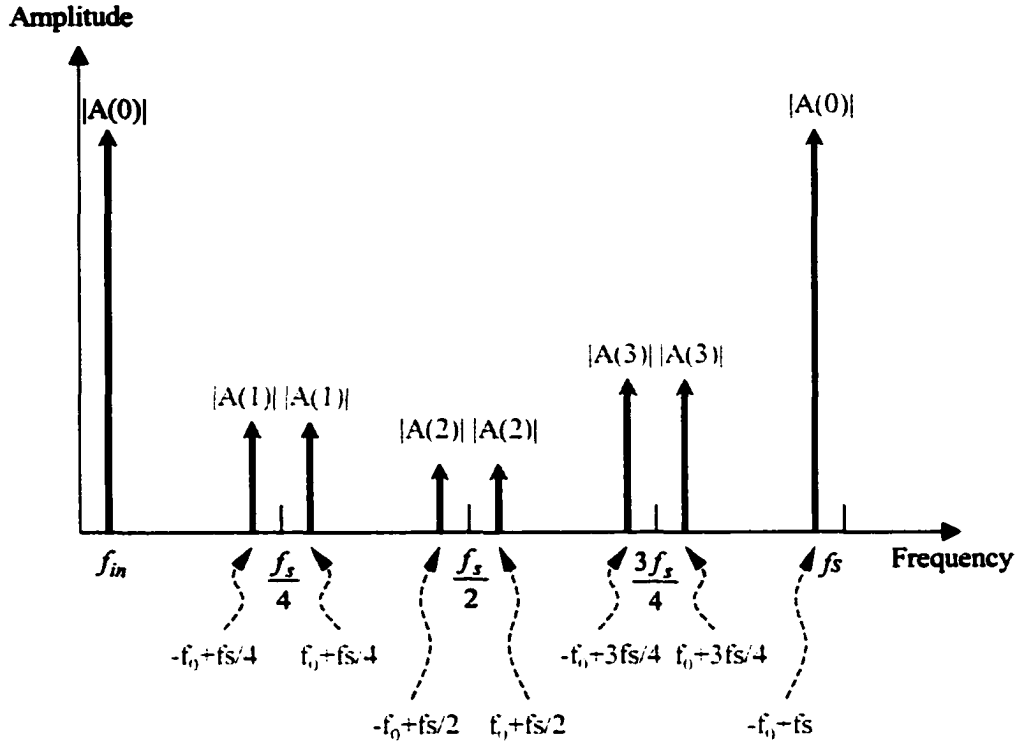


Figure 20 Digital spectrum with gain mismatch

Assume A_m is normally distributed with standard deviation of σ_A and mean of $\overline{A}$. By Parseval's theorem, we have

$$P_1 = \sum_{k=0}^{M-1}|A(k)|^2 = M\sum_{k=0}^{M-1}\left(\frac{A_m}{2M}\right)^2 = \frac{1}{4}\frac{\sum_{k=0}^{M-1}A_m^{\,2}}{M} \approx \frac{1}{4}(\sigma_A^{\,2} + \overline{A}^2) \qquad (44)$$

$$P_2 = \sum_{k=0}^{M-1}|A(k)|^2 \approx \frac{1}{4}(\sigma_A^{\,2} + \overline{A}^2) \qquad (45)$$

The total signal and distortion power is

$$P = P_1 + P_2 = \frac{1}{2}(\sigma_A^{\,2} + \overline{A}^2) \qquad (46)$$

The signal power of the fundamental is

$$|A(0)|^2 = \left|\frac{1}{2M}\sum_{k=0}^{M-1} A_m\right|^2 \approx \left|\frac{1}{2}\bar{A}\right|^2 = \frac{1}{4}\bar{A}^2 \qquad (47)$$

The power of the noise in the range of $(0,1/(2f_s))$ is

$$noise = (P - 2|A(0)|^2)/2 = \frac{1}{4}\sigma_A{}^2 \qquad (48)$$

Assume the gain a_m for each converter is proportional to A_m with constant efficient β, then

$$a_m = \beta A_m \qquad (49)$$

where m=0, ...M-1

So, we have

$$\begin{aligned} \sigma_a &= \beta\sigma_A \\ \bar{a} &= \bar{A} \end{aligned} \qquad (50)$$

Then, the signal-to-noise ratio is

$$SNR = 10\log 10\left(\frac{\frac{1}{4}\bar{A}^2}{\frac{1}{4}\sigma_A{}^2}\right) = 20\log 10\left(\frac{\bar{A}}{\sigma_A}\right) = 20\log 10\left(\frac{\bar{a}}{\sigma_a}\right) \approx 20\log 10\left[\frac{a}{\sigma_a}\right] \qquad (51)$$

From equation (51), we can see that, if the gain mismatch can be decreased by two times, the SNR can be increased by about 6dB. Figure 21 shows the comparison between the numeric results obtained based on equation (51) and the simulated results obtained by averaging 100 arrays. As we can see from Figure 21, the numeric results are very close to the simulated results when the time-interleaved number M is greater than 12. For a four-way, time-interleaved analog array, the signal to noise ratio can be estimated using equation (52).

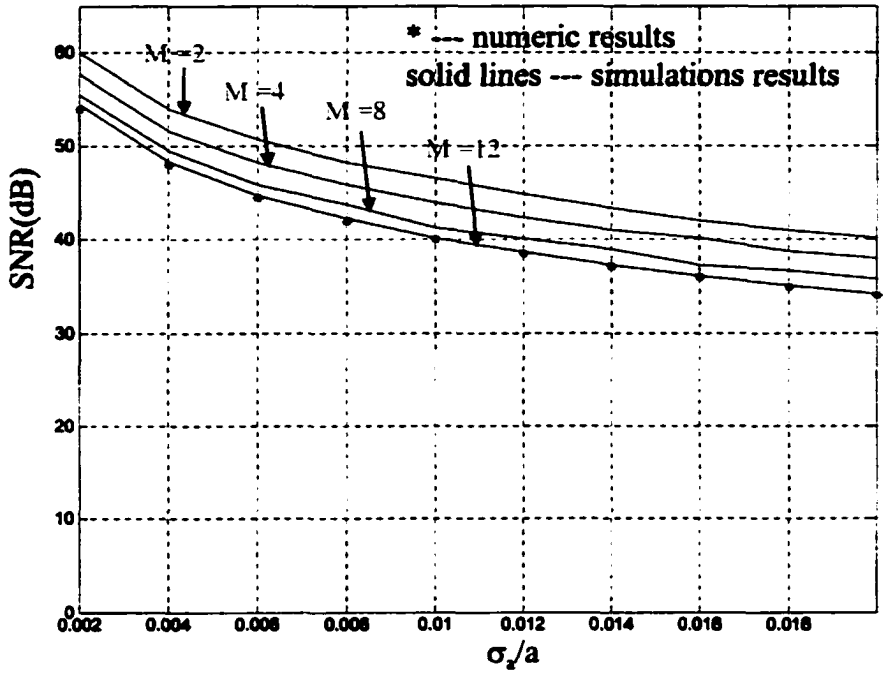


Figure 21 The relationship between SNR and gain mismatch

In order to achieve 6b accuracy, the gain mismatch σ_a / a between channels needs to be smaller than 1.8%.

$$SNR = 20\log 10\left[\frac{a}{\sigma_a}\right] + 3(dB) \qquad (52)$$

4.1.3 Converter offset

Converter offset mismatch can be modeled by simply adding a DC level with the input signal that is unique for each channel. Assuming that for each individual analog channel, the analog input signal is $A\sin(\omega_{in}t) + D_m$, then, the digital spectrum for time-interleaved arrays can be derived.

For a input signal $\sin(\omega_{in}t) + D_m$, the Fourier transform is given by

$$F^a(\omega) = Aj\pi[(\delta(\omega + \omega_{in}) - \delta(\omega - \omega_{in})] + 2\pi D_m \delta(\omega) \tag{53}$$

Substituting (53) into (23), we can derive

$$\begin{aligned} F(\omega) = \frac{1}{T}\sum_{k=-\infty}^{\infty} Aj\pi[\delta(\omega + \omega_{in} - k\frac{2\pi}{T}) - \delta(\omega - \omega_{in} - k\frac{2\pi}{T})] \\ + \frac{1}{T}\sum_{k=-\infty}^{\infty} D(k)2\pi\delta(\omega - k\frac{2\pi}{MT}) \end{aligned} \tag{54}$$

where

$$D(k) = \frac{1}{M}\sum_{m=0}^{M-1} D_m e^{-jkm\frac{2\pi}{M}} \tag{55}$$

It is easily to prove that

$$D(k) = D^*(M-k) \tag{56}$$

So, we have

$$|D(k)| = |D^*(M-k)| = |D(M-k)| \tag{57}$$

The first term in equation (54) is the well-known digital spectrum representation of a uniformly sampled sine wave signal [46]. The second term is the spectra due to analog channel offset mismatch. As we can see from equation (54), the spectra lines due to channel offset mismatch are located at the fraction of the sampling frequency, as shown in Figure 22. This will not degrade the performance of the A/D converter if the tone at fs/4 and fs/2 is not frequency dependent [47]. However, if the channel offset between the arrays is dynamic offset as we discussed before, it will degrade the performance of the composite array.

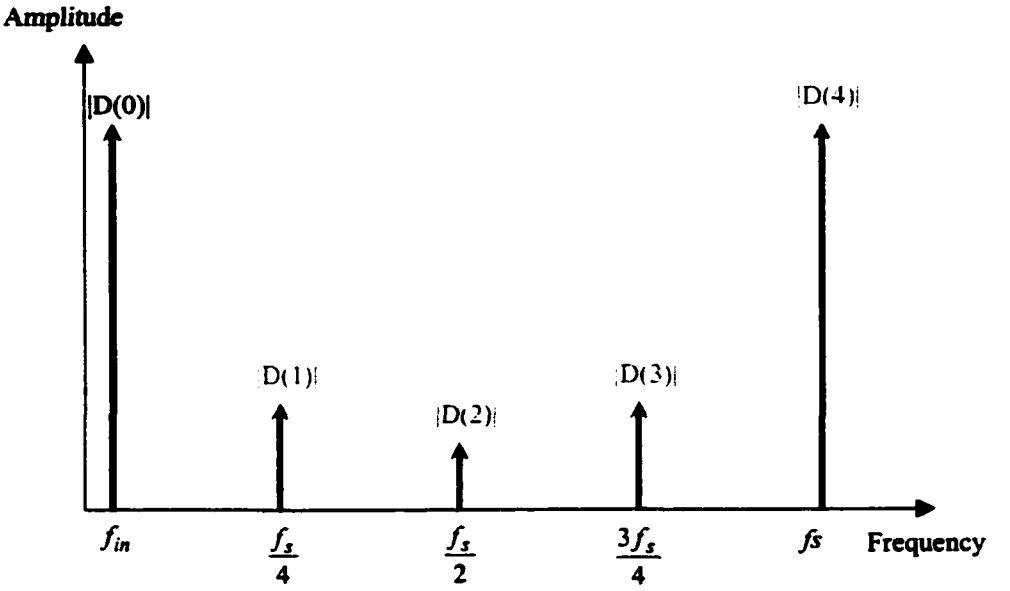


Figure 22 Spectrum with channel offset mismatch

Assume D_m is normally distributed with standard deviation of σ_D and zero mean. The power of the noise in the range of $(0,1/(2f_s))$ is

$$noise = \frac{1}{2}\sum_{k=0}^{M-1} D(k) = \frac{M}{2}\sum_{m=0}^{M-1}\left(\frac{D_m}{M}\right)^2 = \frac{\sum_{m=0}^{M-1} {D_m}^2}{M} \approx {\sigma_D}^2 \qquad (58)$$

The signal power is

$$signal = \frac{A^2}{4} \qquad (59)$$

The signal-to-noise ratio is

$$SNR = 10\log 10\left(\frac{\frac{A^2}{4}}{\frac{{\sigma_D}^2}{2}}\right) = 20\log 10\left(\frac{A}{\sqrt{2}\sigma_D}\right) \qquad (60)$$

Equation (60) implies that if the amplitude of the analog input signal is increased by 2, or the analog channel offset mismatch of the array is decreased by 2, the SNR can be improved by about 6dB.

Figure 23 shows the comparison between numeric results obtained by using equation (60) and the simulated results obtained by averaging 100 arrays using Matlab. Different from the previous two cases, the signal-to-noise ratio (SNR) is not dependent on the number of interleave. As we can see from Figure 23, the curve fit of the numeric results match the simulated results precisely.

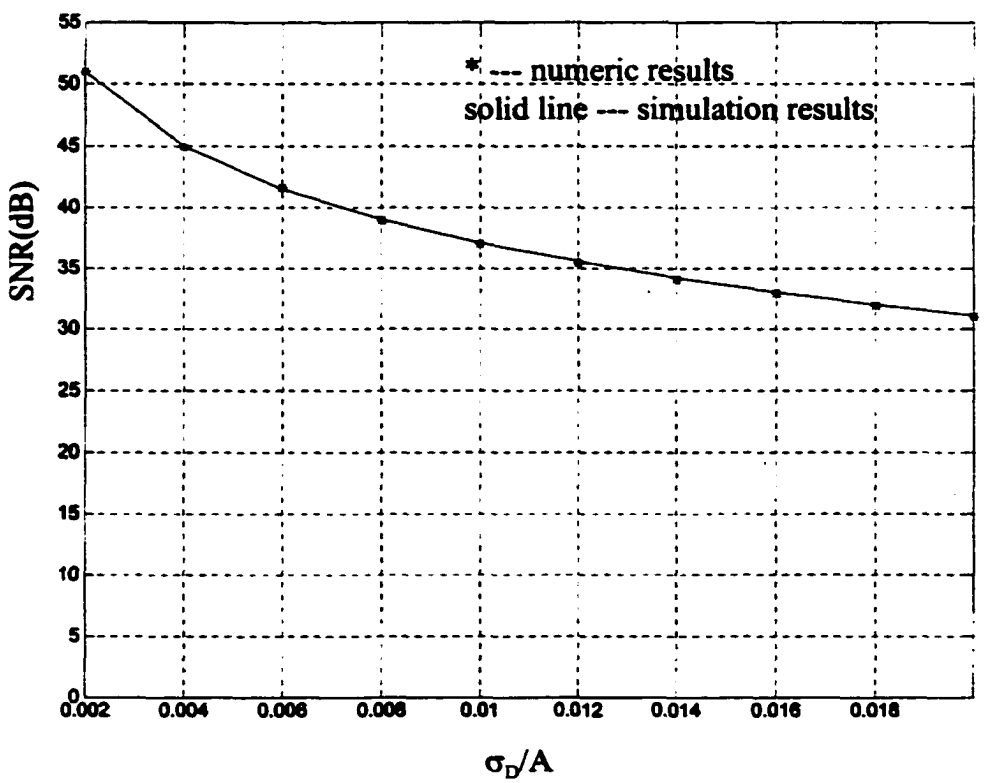


Figure 23 The relationship between SNR and converter offset

4.2 Whole architecture

In Figure 24, the whole scheme is shown. In order to minimize the error introduced by the mismatch between converter arrays, all of the ADCs within the flash array share the same reference resistor string and each comparator shares the same preamplifier stage with the other converters in the array. To a first order, this eliminates variations in reference string and converter offset voltages from degrading performance of the converter array. Additional techniques are used to minimize interaction between converters and to minimize corruption of the input signal by regeneration induced noise. Two chips have been designed to explore

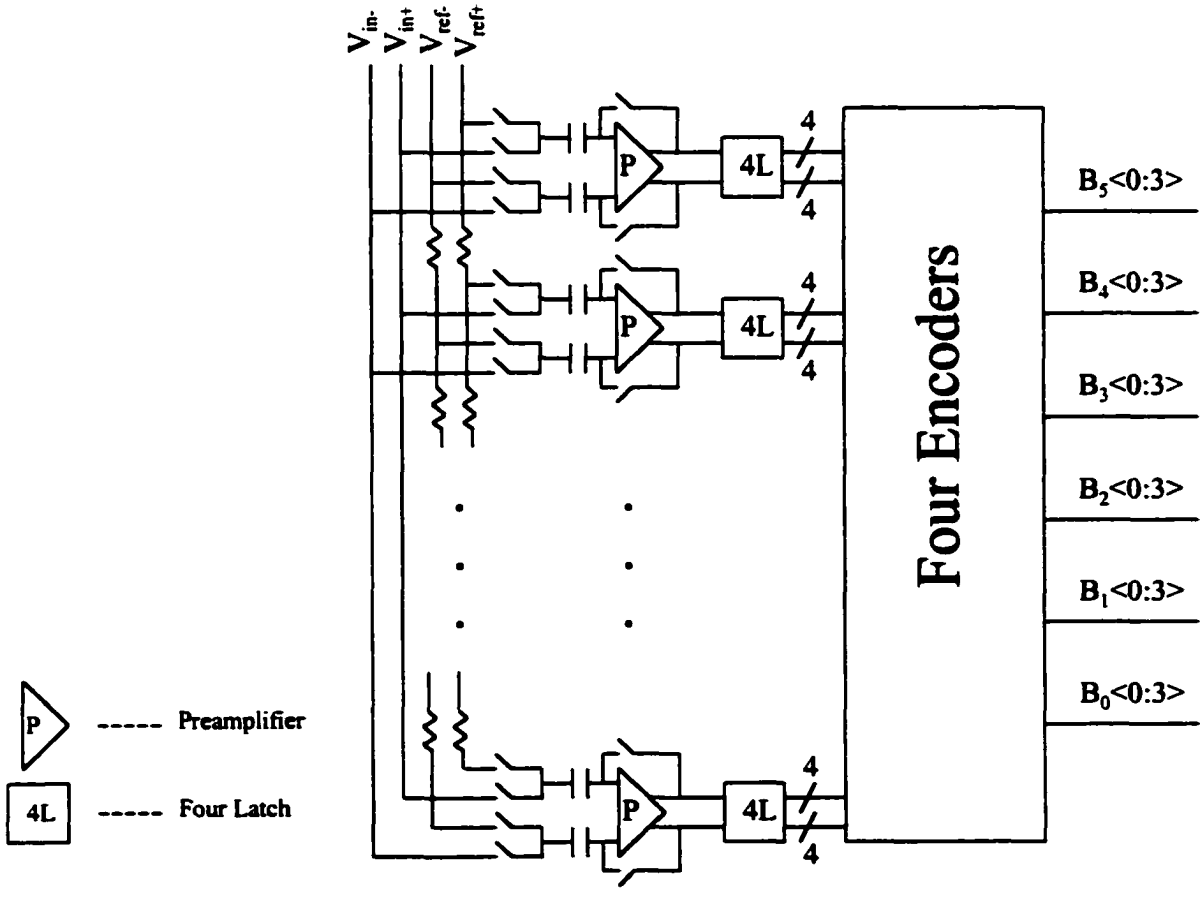


Figure 24 Block Diagram of A/D Converter

this unique idea. The design of these two chips will be explained in detail in this chapter. Figure 24 shows the basic blocks of both chips. However, the regeneration circuitry and clock generator were designed in different ways that will be explained later.

4.2.1 Whole scheme

The simplified block diagram of the A/D converter is shown in Figure 24. At the front end of this A/D converter are 64 comparators that compare the fully differential input signal and the differential reference voltage. This comparator array is followed by the error correction and 'One Of Circuitry' (OOC) that selects one of the 63 possible references as the estimation of the input voltage. The error correction circuitry removes any bubbles that may be present on the thermometer code in order to minimize the possibility of spurious output codes [49]. The output high of the error correction and One Of Circuitry enable one address of ROM to generator a 6b binary output for each channel. Bias reference and clock generator are also implemented on the chip.

4.3 Design of the first prototype

The first prototype was fabricated using a 3.3V digital 0.35 micron bulk CMOS process technology. On this chip, in order to minimize the effect of timing skew effects between converters, all clocks are derived on-chip via PLL (designed by Kae Wong) which is locked to an externally applied 125MHz input clock. Also, provision exists for fine adjustment of individual clocks by an analog input pin associated with each converter.

4.3.1 Preamplifier design

4.3.1.1. Finite bandwidth of preamplifier

The preamplifier can be modeled as a simple low pass filter shown in Figure 25. The transfer function for the preamplifier can be derived as

$$H(S)=\frac{V_0(S)}{V_i(S)}=\frac{1}{SCR+1} \qquad (61)$$

Starting at t=0, a sinusoidal signal is applied at the input

$$V_i(t)=A\sin(\omega_1 t) \qquad (62)$$

Then, at the output we can obtain

$$V_0(S)=\frac{\omega_0}{S+\omega_0}\cdot A\frac{\omega_1}{S^2+\omega_1^2} \qquad (63)$$

and

$$\omega_0=\frac{1}{RC}$$

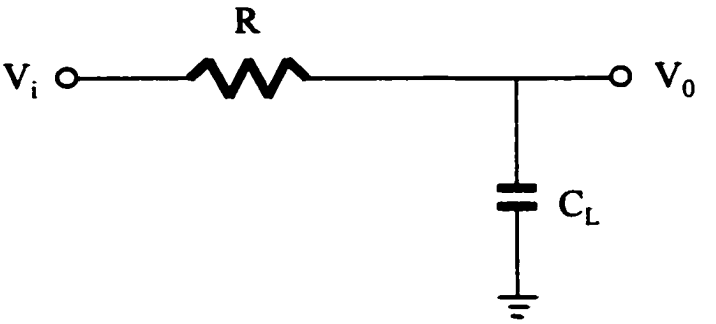


Figure 25 Simplified model of the preamplifier

The transient response at the output is (Appendix A)

$$V_0(t) = A\frac{\omega_0\omega_1}{\omega_1^{\,2}+\omega_0^{\,2}}e^{-\omega_0 t} + A\frac{\omega_0(\omega_0\sin(\omega_1 t)-\omega_1\cos(\omega_1 t))}{\omega_1^{\,2}+\omega_0^{\,2}} \qquad (64)$$

Equation (64) can be rewritten as

$$V_0(t) = A\frac{\omega_0\omega_1}{\omega_1^{\,2}+\omega_0^{\,2}}e^{-\omega_0 t} + A\frac{\omega_0}{\sqrt{\omega_1^{\,2}+\omega_0^{\,2}}}\sin\left[\omega_1 t - \tan^{-1}\left[\frac{\omega_1}{\omega_0}\right]\right] \qquad (65)$$

From equation (65), we can see that the first term on the right side is an error term due to finite acquisition time. And it approaches zero when time increases. Due to the finite bandwidth of the preamplifier, both amplitude and phase are modulated by the preamplifier, which is the second term on the right side. Now, let us find out the bandwidth of the preamplifier in order to have 6b accuracy.

To achieve n-bit accuracy, the following condition needs to be met.

$$A\left[1-\frac{\omega_0}{\sqrt{\omega_0^{\,2}+\omega_1^{\,2}}}\right] < \frac{A}{2^n} \qquad (66)$$

For a 6b Nyquist rate analog-to-digital converter with sampling frequency of 500MS/s, when the analog input frequency ω_1 is equal to 2π x 250MHz , in order to achieve 6b resolution, the 3dB bandwidth of the preamplifier ω_0 needs to be greater than 1.4GHz.

4.3.1.2 Circuit design

The schematic of the preamplifier is shown in Figure 26 along with the associated switch phasings. The input differential pair M_1 and M_2 is used with a pair of sampling capacitors,

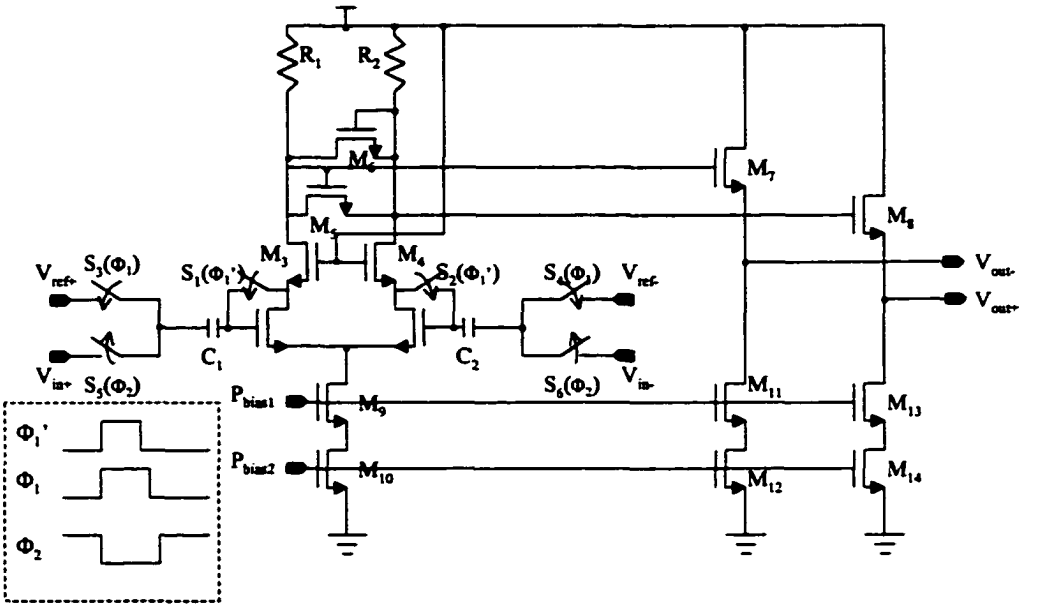


Figure 26 Preamplifier schematic and auto-zeroing timing

which periodically sample and store the preamplifier offset voltage [11]. M_3 and M_4 are isolation transistors that decrease the kick-back to the input from the following regeneration stages and transistors M_5 and M_6 are used to limit the output swing. The loads of the input differential pair are well resistors R_1 and R_2, which results in lower harmonic distortion than an active load [11]. S_1 and S_2 are the switches for auto zeroing, which only occurs at about every 400 usec. By doing this, auto zeroing will not limit the conversion speed of the ADC comparing with conventional implementations, which performs the auto zeroing before every comparison [40][41]. During this period, switches S_3 and S_4 are closed to sample the reference voltage V_{ref+} and V_{ref-}. In order to decrease the charge feedthrough due to switches S_1 and S_2, the switches S_1 and S_2 are opened earlier than switches S_3 and S_4 which connect to the voltage reference. Switch S_5 and S_6 are not closed until all other switches are open. Source followers M_7 and M_8 further isolate any kick-back and shift the DC level.

4.3.2 Latch design

The schematic of the first comparator latch (latch1) is shown in Figure 27. All four channels of latches share the same input differential pair, which in turn is driven by a single preamplifier. With proper timing, the tail current flow through transistors M_{19} and M_{20} is nearly constant, which minimizes kick-back noise from the regenerators. Sharing of the input differential pair by all the latches also significantly reduces the effects of device mismatch on overall converter array performance. At any one time, two of the PLL generated clock signals V_{bias1}, V_{bias2}, V_{bias3} and V_{bias4} are high, which means two channels are in track mode while the other two channels are in latch mode. By doing this, we can ensure the constant current mode operation, which is very important to reduce the noise on chip [42].

The schematic of the second stage latch (latch 2) is shown in Figure 28. When CLK goes

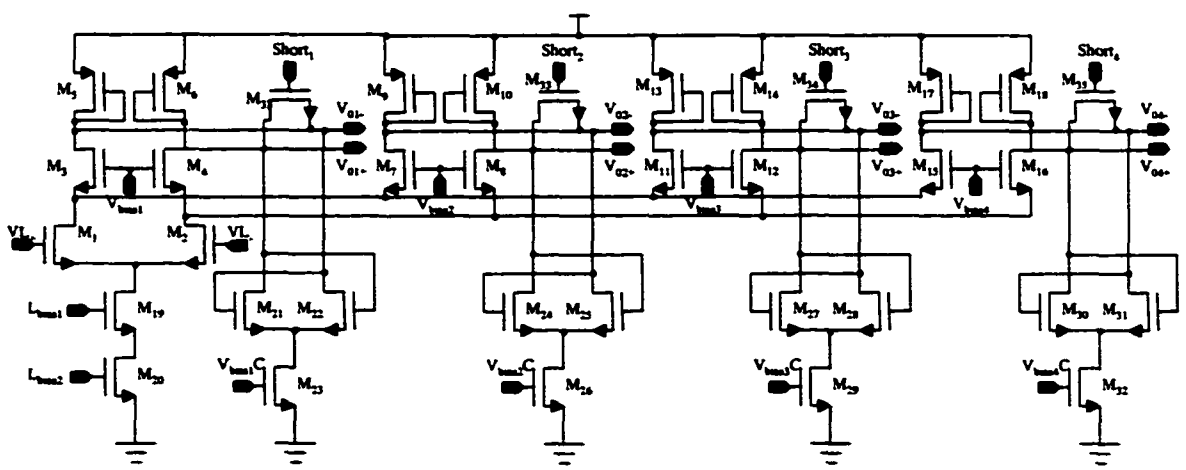


Figure 27 Schematic of latch1 with all 4 channels

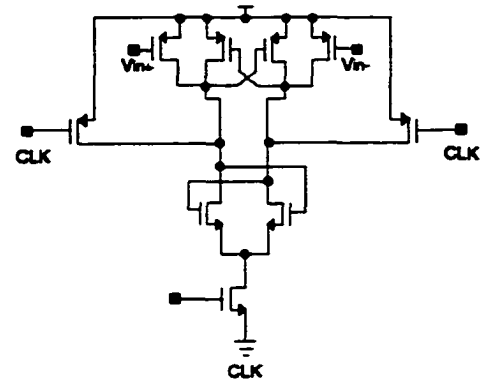


Figure 28 The schematic of latch2

high, the output goes to VDD to minimize hysteresis. In order to minimize the possibility of upsetting latch1, latch2 is regenerated one quarter of a clock cycle after latch1 regenerates.

Timing is very critical in this strategy. In order to minimize the timing skew between the channels, the clocks are distributed using a tree structure, which results in nearly equal propagation delay to all switches and latches in each of the four converters. The error correction circuitry is used to remove any bubbles in the thermometer code prior to encoding. After the error correction circuit, the transition point is detected by the so called one of circuits or 'OOC'. The high output of the OOC will enable one address of ROM, which is programmed with a modified quasi-Gray code. The modified quasi-Gray code is similar to a conventional Gray code, but it may be converted to a binary code with only a single gate at the output of the ROM. A fast-switching low power ROM architecture is used here similar to that described by Deevy [50] which requires almost no current under static condition and does not require a precharge mechanism. The design of the digital encoder will be discussed later in detail.

4.3.3 Performance analysis

4.3.3.1 Simulation result

The whole scheme was simulated using HSPICE within the Cadence environment and shows good performance at sampling frequency of 500MS/s. It achieves higher than 5.5 ENOB up to Nyquist rate. Even though it was tested under no mismatch and no noise condition in Cadence, switch injection might cause degradation of the performance. The setup for testing in Cadence is shown in Figure 29. As shown in this figure, the four channel outputs go through a high speed 'MUX' to be combined as one channel of 6-bit digital output. Then, the digital signal is converted to an analog signal by an ideal digital-to-analog converter. After that, the data were processed using Matlab.

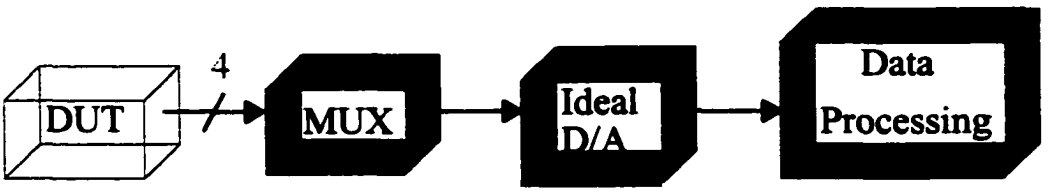


Figure 29 Simulation test setup

4.3.3.2 Testing result

The chip was fabricated using HP 0.35μ CMOS technology. A die photograph of the chip is shown in Figure 30. The total die size including pads and various test circuitry is 3.3mm x 2.4mm This chip was tested using a Tektronix TLA 700 series logic analyzer that is synchronized to the chip output data enable signals.

Figure 31 shows the testing result from the logic analyzer. The sampling frequency was running at 500Msample/s and the analog input frequency is at 1.3MHz. As we can see in Figure 31, the output of the four channels are synchronized. The data from the Logic Analyzer were exported to the PC and analyzed. By doing Fast Fourier Transform (FFT), it turned out that the effective number of bits (ENOB) of each separate channel is about 4.1 and the ENOB of the combined four channels is only 2.5, which is 1.5 bit less than that of the each channel. The mismatch between the channels degrades the chip performance a lot. After debugging the chip, several error sources that degraded the performance of the chip were discovered.

One thing that we found was that the multi-phase clocks from the clock generator had relatively high clock skew and each clock had relative high jitter. As we discussed earlier, the clock skew will contribute tones at fs/2 and fs/4, which will degrade the combined performance. Clock jitter will raise the noise floor and degrade the performance of each channel and the performance of the whole chip. There are many error sources that contributed to the clock jitter and the multi-phase clock skew. First, is substrate noise. The digital part of the system generated a lot of noise which disturbed the clock generator and degraded the jitter performance of the clock Second, it might be the clock generator design itself. For clock skew, mismatch between the delay cells in PLL would contribute to clock skew. Since it is very difficult to design the clock generator to have low jitter and low skew based on PLL on the noisy substrate, a simple technique was proposed for this work which will be explained later.

From the digital output captured by the logic analyzer, bumps around the midrange at the zero crossing of the sine wave were observed. This was suspected to be caused by the folding structure that was employed in the layout. In order to increase the matching performance of the resistor string for the reference, a folding structure was used for the resistor string which generated the reference. However, this caused a long delay of the signal from the comparators to the input of the encoder around midrange. Because of this, it might cause encoding error.

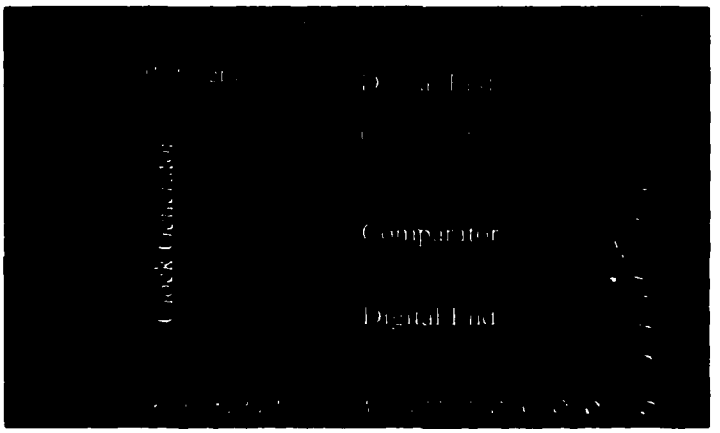


Figure 30 Die photograph

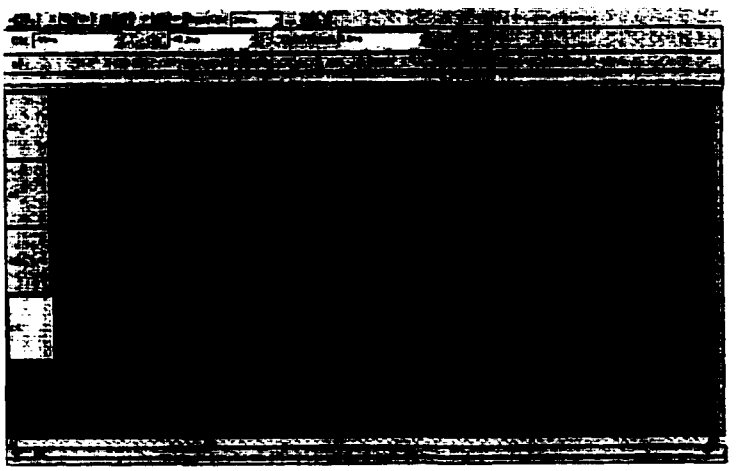


Figure 31 Testing result from Logic Analyzer

4.4 Prototype of the second chip

In this section, the prototype of the second chip is discussed. As we mentioned before, it is very difficult to design a low jitter and low skew clock generator in such a noisy substrate, so a simple design is proposed to generate low jitter and low skew multi-phase clocks.

4.4.1 Multi-phase clock generator

4.4.1.1 Scheme

Employing time-interleaved technology into a FLASH architecture, very high speed ADCs can be designed. However, the high speed sample and hold always is the bottleneck to the speed of ADCs. Without a sample and hold, low jitter multi-phase clock generators are required in order to have good performance for ADCs. A simple and unique precise multi-phase clock generator is proposed.

As we all know, a low jitter clock generator is critical in Nyquist data converter design. For 6 bits 500Ms/s flash converter, 20ps clock jitter will introduce 1 bit error to the system. So, a precise multi-phase clock generator is very crucial to achieve high performance. One possible way to implement multi-phase clock generator is by using PLL or DLL. However, mismatch between the delay cells will introduce systematic phase skew. Indeed, it is difficult to design even a single phase clock that will meet these jitter requirements.

Figure 32 shows the whole scheme of the clock generator. At the front end is a Sine Wave Shaper that is a fully differential preamplifier to obtain high noise rejection. The Sine

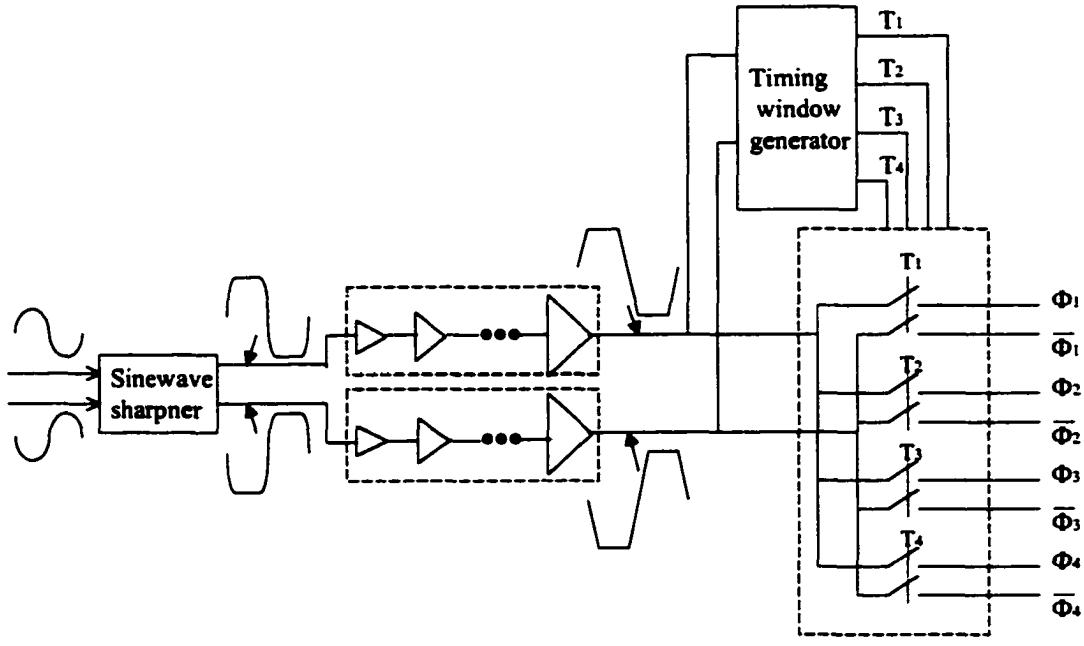


Figure 32 Block diagram of multi-phase clock generator

Wave Shaper has a DC gain of 4. After that, a buffer chain is used to further sharpen the rising and falling edge of the clock. These two complenentary clocks are the input of the timing window generator, which generate four different timing windows to control the switches. The timing window generator consists of two fully differential flip-flops connected as a divide-by-four Johnson counter[19]. Figure 33 shows the detail of the timing window generator. As we can from this figure, the two fully differential flip-flops cross coupled connected as a divide by-four Johnson counter. The timing window clock relative to the input clock is shown in Figure 34. Each timing window will pick one pulse out of four pulses. The frequency of each of the four clocks, Clk_1, Clk_2, Clk_3 and Clk_4 is only ¼ of the original clock signal Clk.

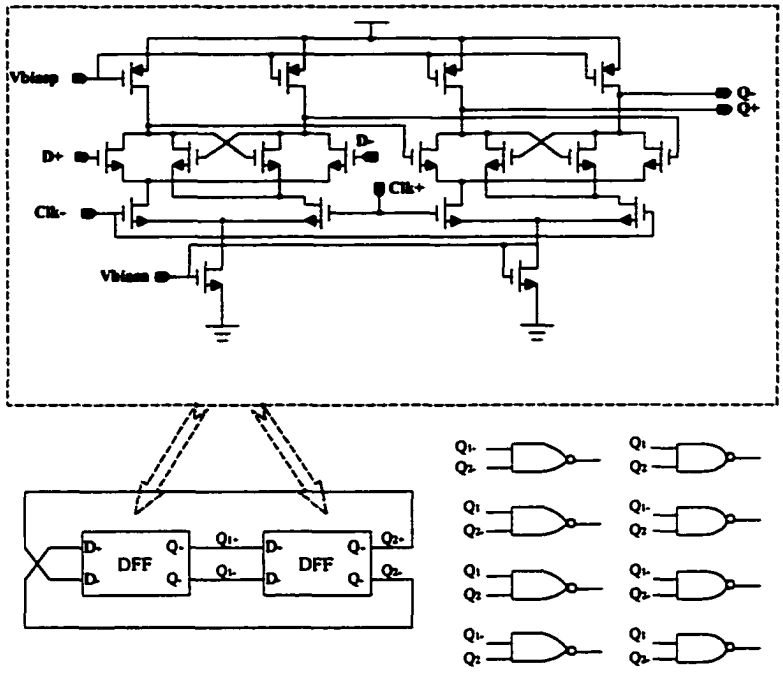


Figure 33 Timing window generator

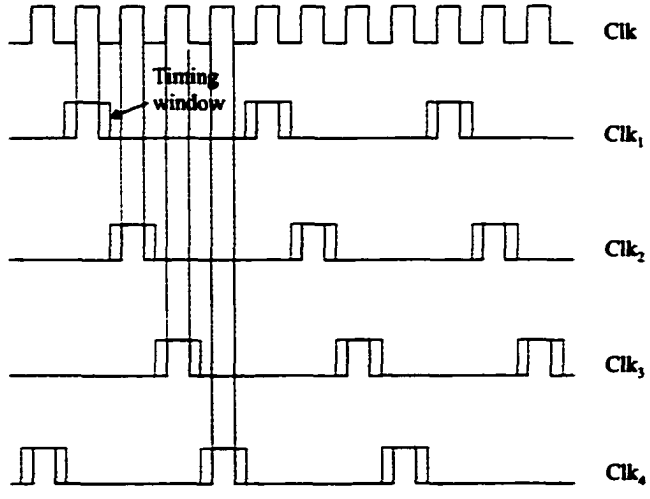


Figure 34 Timing window relative to each individual clock

4.4.1.2 Jitter analysis

A useful approximation that is frequently employed in jitter analysis is "first crossing approximation" [51], and is illustrated in Figure 35. Assuming possible voltage error at zero crossing is ΔV_n, then the timing error at the zero crossing point is given by ΔV_n devided by the slope at that point shown in equation (67).

$$(\Delta t)_{rms} = \sqrt{\frac{\overline{\Delta V_n^{\,2}}}{(slope)^2}} \qquad (67)$$

As we can easily see from equation (67), the higher the slope, the less the timing error with the same amount of voltage error. By using the first crossing approximation, we can predict the minimal timing jitter of the sine wave. As we know, the sine wave has the highest slope at the zero crossing, which is shown in the following equation.

$$slope_{\max} = 2\pi fA \qquad (68)$$

where f and A is the frequency and amplitude of sine wave. By having the Sine Wave Shaper at the input in the clock generator, the slope of the signal at the zero crossing point is increased by the DC gain, which implies that the jitter will equivalently decrease by the DC gain of the Sine Wave Shaper. Then, a chain of buffers follow the sine wave shaper to further decrease the rising and falling time of the signal with the high gain of the buffer at the trip point. The buffers are properly sized to optimize the driving capability and balance the rising edge and falling edge. As we mentioned before, multi-phase clocks with less than 20ps are required as they are to be used in 6 bits 600Ms/s Nyquist rate converters. In this clock generator, there are two main error sources. One error source is in the Sine

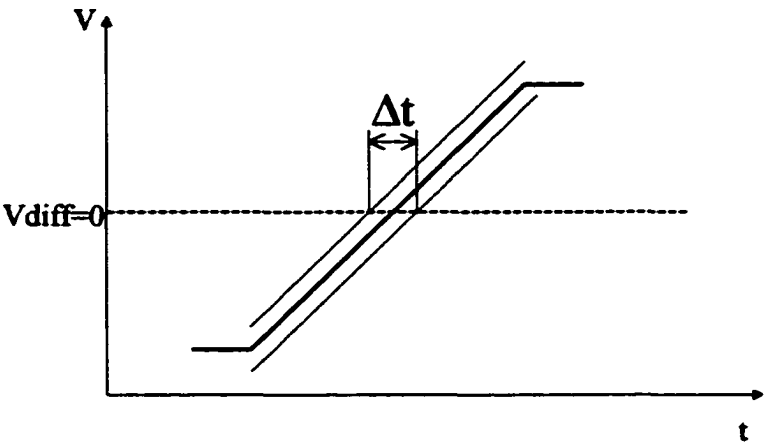


Figure 35 The relation between the voltage noise and timing jitter

Wave Shaper and buffer chain. In order to suppress the jitter, a low noise power supply and quiet ground are required. Also, fast rising and falling clock edges will help to keep the timing jitter low. The second error source comes from the mismatch between the switches. Careful layout is needed to minimize the mismatch between the switches and propagration delay.

4.4.2 Comparator design

Each comparator consists of a preamplifier and two stages of regeneration. All four channels share a single preamplifer with a gain of about 5. The reference strings are shared by all channels to minimize the mismatch between channels. As shown in Figure 36, all four channels share a single preamp with a gain of 10. Clock signals az1, az2 and az3 are clock zeroing, which only occurs about every 400usec. During auto zeroing, the preamp offset voltage will be sampled and stored. Offset mismatch between channels will decrease by the

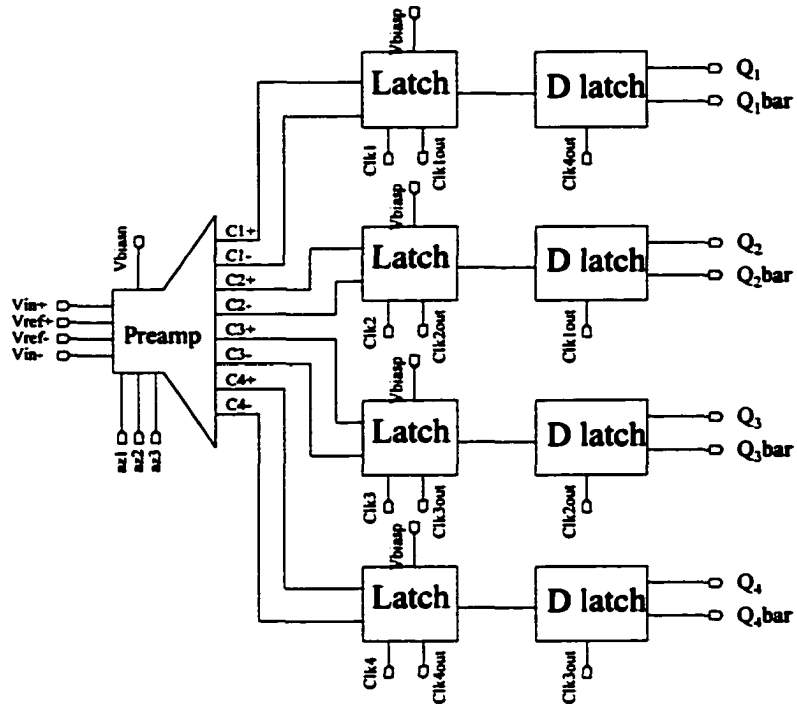


Figure 36 The schematic of the comparator

gain of the preamp, which is about 10. Clk1, Clk2, Clk3 and Clk4 are clocks generated from the multi-phase clock generator. Clk1out, Clk2out, Clk3out and Clk4out are buffered clocks of Clk1, Clk2, Clk3 and Clk4, which are used to trigger D latches that happen at the end of the regeneration cycle of the previous latch. The layout of the comparator is shown in Figure 37. As we discussed, it includes one preamplifier, four latches and four D latches. In order to simplify the layout procedure, the comparator was designed so that sixty-three comparator cells may be placed adjacent to each other without additional global routing in terms of power supply, ground and substrate tie. By doing this, the whole layout procedure was simplified and more efficient.

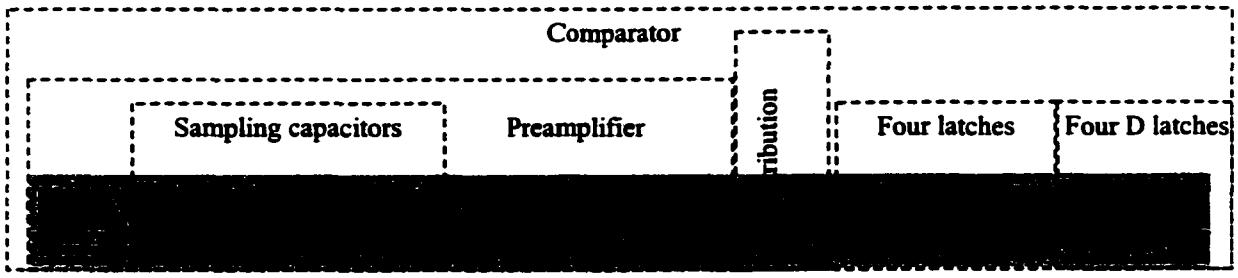


Figure 37 Layout of the comparator

4.4.2.1 Preamplifier design

The schematic of the preamplifier is shown in Figure 38 along with the associated switch phasing. This preamplifier has two stages. The goal is to achieve high gain and high bandwidth. The preamp achieves a -3dB bandwidth of 1.5GHz based on simulation. The first stage is used with a pair of sampling capacitors, which periodically sample and store the preamplifier offset voltage[11]. Source followers are used to isolate the inference between different channels and shift the DC level. S_5 and S_6 are the switches for auto zeroing, which only occurs about every 400usec. During this period, switches S_1 and S_2 are closed to sample the reference voltage V_{ref+} and V_{ref-}. In order to decrease the charge feedthrough due to switches S_5 and S_6, the switches S_5 and S_6 are opened earlier than switches S_1 and S_2 which connect to the voltage reference. Switches S_3 and S_4 are not closed until all other switches are open. During auto zeroing, the sampling capacitors C_1 and C_2 help to stabilize the feedback loop. The capacitor value of C_1 and C_2 are carefully chosen to guarantee enough phase margin and to ensure adequate matching performance. In order to achieve high density, the

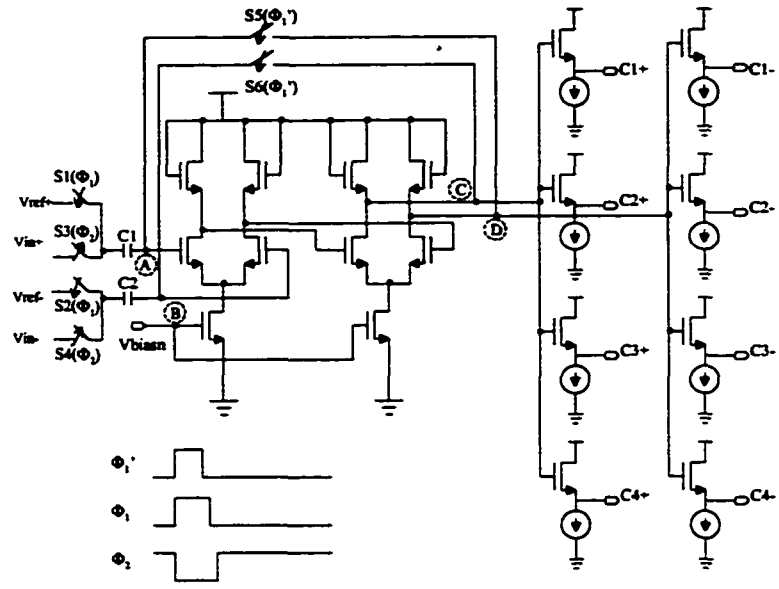


Figure 38 Schematic of the preamplifer

capacitors are implemented using metal 1, metal 2, metal 3 and metal 4 that are connected as a sandwich structure.

Since the preamplifier amplifies the analog signal before regeneration. Any mismatch due to layout will introduce extra error into the system. The layout of the preamplifier was done very carefully. Figure 39 shows the layout of the preamplifier. In the schematic, signals at nodes C and D will be distributed equally to the source followers. Tree structures are used to

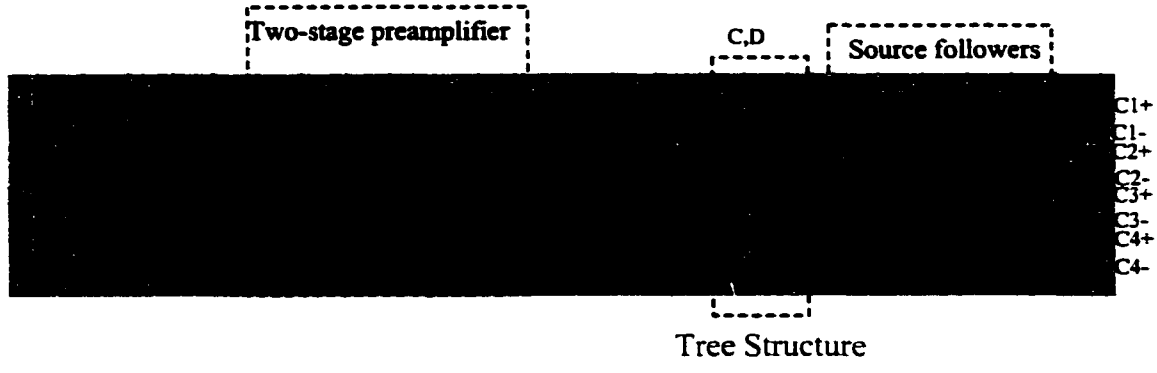


Figure 39 Layout of the preamplifier

maintain equal propagation delay. The two-stage preamplifier was placed symmetrically to minimize the mismatch between the channels.

4.4.2.2 Comparator latch design

Switches S_1 and S_2 are controlled by sampling clock SH. When SH goes high, both switches will be turned on. The differential signals from preamp will be sampled on the gates of M_{10} and M_{13}. At the same time, transistors M_7 and M_8 will be turned on and transistors M_5 and M_6 will be turned off. The voltages at nodes A and B will be pulled up to VDD by transistors M_7 and M_8. During this time, the latch is being reset. When SH goes low, switches S_1 and S_2 will be turned off. The input signal will be stored on the gate of M_{10} and M_{13}. The change at the input will not effect the latch decision. Then, transistors M_7 and M_8 will be turned off and transistors M_5 and M_6 will be turned on. The latch then starts to regenerate the differential signal. The time-interleaved structure relaxes the timing requirement of each

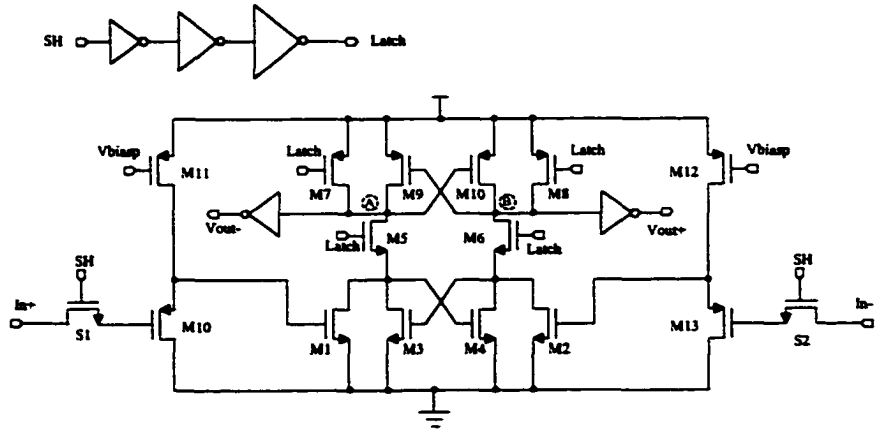


Figure 40 Schematic of comparator latch

channel. For a four-array time-interleaved structure, each converter array works at one fourth of the combined speed. Hence, the comparator latch will have about 4x the time to regenerate the signal compared to a single channel system. When switches M_5 and M_6 are turned off, the charge injection noise will be coupled to the gates of transistors M_1 and M_2 that potentially steer the latch to the wrong direction in regard to the input signals. Sources followers M_{10} and M_{13} provide a low impedance path to minimize this effect so the signal sampled onto the gates of transistors M_{10} and M_{13} in only minimally disturbed by the charge injection noise. Source followers M_{10} and M_{13} also shift the DC level of the input. After this latch, the digital output will be stored in a conventional D latch prior to digital processing.

4.5 Power supply and ground noise consideration

As we discussed before, the power supply noise and ground bounce will introduce timing jitter to the multi-phase clock, which will raise the noise floor of the reconstructed output spectrum. Power supply noise and ground noise will appear as common mode noise for sensitive analog circuitry, such as the preamp. Depending on the circuitry common mode rejection, it may also appear as comparator offset. If the power supply noise and ground bounce are too high, it will significantly compromise the system. So, power supply noise and ground bounce need to be carefully considered. Where do supply noise and ground bounce come from? It can be explained using a simple inverter.

Figure 41 shows a simple inverter with its load capacitor. L_1 and L_2 are equivalent parasitic inductors combining both bonding wire and package lead. For a regular package such as a PGA, it could be as high as 6nH. When signals at the input go from low to high, the output will go from high to low. Load capacitor C_L will discharge through transistor M_2 and inductor L_2. Since the discharge current is not constant, it will introduce voltage drop ΔV across parasitic inductor L_2. It has the following relation with L_2 and discharge current $i_{discharge}$.

$$\Delta V = L_2 \frac{di_{charge}}{dt} \qquad (69)$$

Hence, the voltage drop ΔV across inductor L_2, on chip ground B is not constant with the voltage at node B being VSS+ΔV. This is often called ground bounce. From equation (69), we can try to find several ways to minimize the ground bounce, substrate noise and power supply noise.

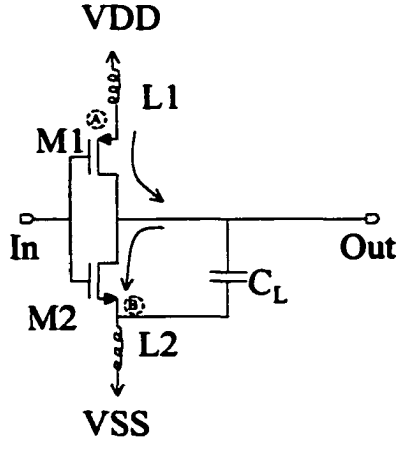


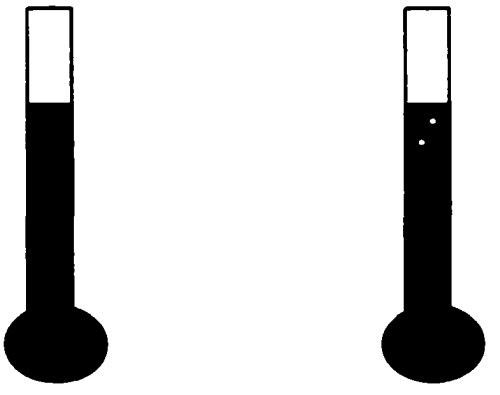
Figure 41 Ground bounce and power supply noise

1) A package with less parasitic inductance should be used. Or chip-on-board in which the die is bonded directly on board to avoid package lead inductance. By doing these, the parasitic inductance L_2 can be minimized which implies less ΔV.
2) From a circuit design stand point, we should try to slow down the clock rising and falling edge, which will decrease $di_{discharge}/dt$. Constant current mode circuitry could also help to decrease ground bounce. Due to constant current mode operation, ideally $di_{discharge}/dt$ would be zero, which implies zero ground bounce.
3) We should try to keep signals fully differential on chip to minimize ground bounce and its effect. Since for fully differential structure, the charge injected into the substrate or power supply will be balanced by the same amount of charge being withdrawn.
4) On-chip decoupling capacitors are favored in the point of minimizing the ground bounce, substrate noise and power supply noise. Decoupling capacitors act as a local 'charge reservoir'. On-chip capacitors are more effective in minimizing power supply noise compared with off-chip capacitors because of the small interconnect inductance and good high frequency performance.

CHAPTER 5 DIGITAL CIRCUITRY AND SIMULATION RESULTS

5.1 Error correction

As we discussed before, for an ideal flash converter, the output of the comparators will be in the term of a "thermometer code". All zeros are above the input voltage and all ones are below the input voltage (shown in Figure 42 (a)). The transition from '1' to '0' can be detected and is easily translated into binary code. However, in reality, time skew and comparator offset may introduce ones within the zeros or vice versa. (shown in Figure 42 (b)). Errors of this type are referred to as "bubbles". By using a simple two-input NAND or



(a)Ideal (b)Reality

Figure 42 Bubbles in thermometer code

NOR gate to detect the transition from '1' to '0', the output 'high' will enable a single ROM word line. With "bubbles" in the outputs from the comparators, more than one transition will be detected this way, which means that more than one address line will be enabled. This will cause dramatic errors at the binary output.

In this design, error correction circuitry is used to remove "bubble" before detecting the '1'/'0' detection [49]. The error correction scheme used here was proposed by Christopher W. Mangelsdorf. " The error correction scheme in the present circuit may be thought of as a voting process. Each comparator output is examined relative to its two nearest neighbors, and the output is changed if it disagrees with both." [49]

The comparator output will be corrected based on the following equation.

$$C_2^* = C_1 \cdot C_2 + C_2 \cdot C_3 + C_1 \cdot C_3 \qquad (70)$$

Where C_2* is the corrected comparator output, C_1 and C_3 are adjacent comparator outputs. If C_2 disagrees with both C_1 and C_3, which means it is " bubble", it will be corrected. For example, if the output of C_1, C_2 and C_3 are '0', '1', '0', then the middle '1' is a "bubble" between ones. Through equation (70), it will be corrected as '0'. If the output of C_1, C_2 and C_3 are '1', '0', '1', then the middle '0' is a "bubble" that needs to be removed. The "bubble" removal is shown in Table 4. After correction, it will be corrected as '1'. After error correction, most common "bubbles" will be removed. Then, the detection of the transition from '1' to '0' can take place. The output of the detection circuitry will enable one address of ROM. However, there are some extreme cases in which "bubbles" can't be removed by error correction as shown in Table 5.

Table 4 Bubble removal

	Case 1		Case 2		Case 3	
	Before Correction	After Correction	Before Correction	After Correction	Before Correction	After Correction
	0	0	0	0	0	0
C_1	0	0	1	0	1 Bubble	1
C_2	1 Bubble	0	0 Bubble	1	1 Bubble	1
C_3	0	1	1	1	0	1
	1	1	1	1	1	1

Table 5 Extreme case where the bubble can't be removed

	Case 1	
	Before Correction	After Correction
	0	0
C_1	1	0
C_2	0 Bubble	1
C_3	1	0 Bubble
C_4	0 Bubble	1
	1	1

In Table 5, an extreme case is shown where the bubble can't be removed even after the bubble removal circuitry. Fortunately, because of the coding method used in the ROM encoder, the "bubble" left in the thermometer code would not cause dramatic error in encoding. We will explain this in the next section.

5.2 ROM encoder

5.2.1 Modified quasi-gray code

Converting the one-to-zero transition point directly into standard binary code may result in large errors in the digital output when two or more transition points exist in the thermometer codes generated by the array of the comparators. As we discussed before, even though bubble removal circuitry can remove the bubbles in some case, there are still some extreme cases in which the bubbles still exist. When multiple transition points appear in the thermometer code, encoding errors can be dramatically reduced by using some type of error-reducing intermediate code [52]. One of the common error-reducing code is the gray code, in which only one bit is allowsed to change between adjacent digital codes. The modified quasi-gray code scheme not only has the quasi-gray code advantage, it also has less gate delay when converting the modified quasi-gray code into binary code [52]. Sixty four possible modified quasi-gray codes will be stored in ROM. Based on the detection circuitry, one address of the ROM will be enabled and encode the thermometer code into binary code. An algorithm for converting a modified quasi-gray code into binary code is shown in equation (71). The modified quasi-gray codes corresponding to the decimal codes from one to seven are shown in Table 6.

$$\begin{aligned} b_n &= c_n; \\ b_i &= c_i \oplus c_{i+1}; \\ b_0 &= c_{0;} \end{aligned} \qquad (71)$$

where n is in the range of (1, n+1).

Table 6 3-bit modified quasi-gray code

Decimal	Quasi-gray
0	000
1	001
2	010
3	011
4	110
5	111
6	100
7	101

5.2.2 Low power ROM encoder

A fast-switching and low power ROM encoder is used. It not only has a low power advantage, it can also prevent sparkle errors by proper sizing of the transistors [53]. In Figure 43, a simplified ROM encoder is shown. All the modified quasi-gray codes are stored in ROM. The drain of the transistor will be tied to high if '1' is stored, or the drain of the

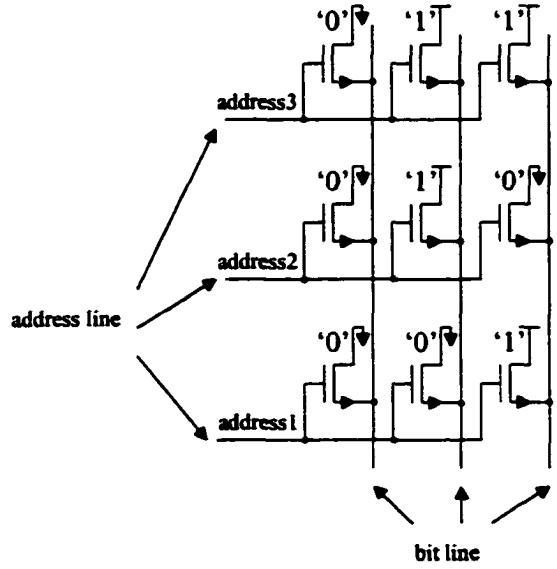


Figure 43 ROM encoder

transistor will be tied to low if '0' is stored. Unless the address line is enabled, the bit cells will not draw any current ensuring low power operation. If both $address_2$ and $address_3$ are enabled, the output would be well defined instead of "can't be decided" because the pull down transistors have two times the W/L of the pull up transistor.

5.3 Simulation result

The whole scheme was simulated using HSPICE within the Cadence environment and shows good performance at fs=500MHz. The setup for testing in Cadence is shown in Figure 29. The output data from the ideal digital-to-analog converter were processed using Matlab. After FFT, SNDR can be calculated. Figure 44 shows the simulation SNDR versus the input frequency at a sampling frequency of 500MS/s. As we can see, SNDR of the ADC is higher than 35.5dB at the Nyquist rate.

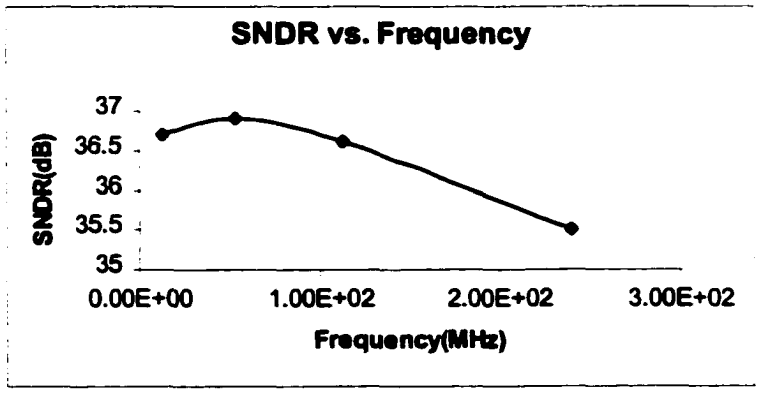


Figure 44 Simulated SNDR vs. Frequency at fs=500MHz

CHAPTER 6 LAYOUT CONSIDERATION

6.1 Floorplan

The overall chip floorplan is shown in Figure 45. As we discussed before, the comparator cell design is done in such a way that the sixty-three comparator cells are easily stacked in a single column. The power lines, n-well ties and substrate ties are running through each cell to ensure low impedance connections. The main power lines are placed both at the top and bottom and are designed to be wide enough to avoid metal migration.

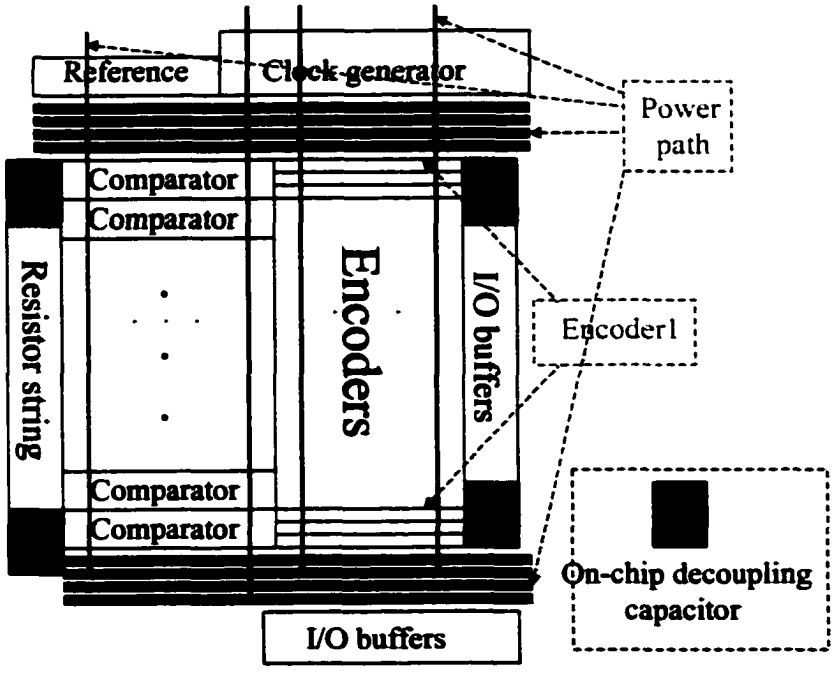


Figure 45 Floorplan

6.2 Noise suppression

As we discussed before, careful design can minimize the power supply noise and ground bounce. Careful layout considerations are also required to suppress the power supply noise, ground bounce and interference in order to achieve high performance. Figure 46 shows the die photo of the whole chip with active area of 2.08 mm^2. Since an A/D converter is a mixed signal system, careful partitioning is required during layout to minimize the interference between sensitive analog circuits and noisy digital circuits. Analog inputs are separated from noisy pins by pins dedicated to the power supply or ground. In the layout, shielding has been used where noisy clock lines are running through sensitive analog signals, such as the output signals of the preamplifiers before latches.

As many pins as possible have been dedicated to power supply and ground to reduce the parasitic inductance due to bonding wires and package leads. Also, on chip de-coupling capacitors (about 1nF) are added to further minimize the power supply noise and ground bounce. Since the process that we used is a high impedance substrate process, noisy digital circuits are placed far apart from the sensitive analog circuits to help minimize the interference through the substrate [54]. Large output buffers are placed as far from the analog circuits as possible. A loop of guard ring is place around the digital circuits to collect the substrate noise generated by noisy digital circuitry. The substrate and guard ring are tied to dedicated quiet pins and as many pins as possible are dedicated to substrate ties in order to suppress substrate noise [55].

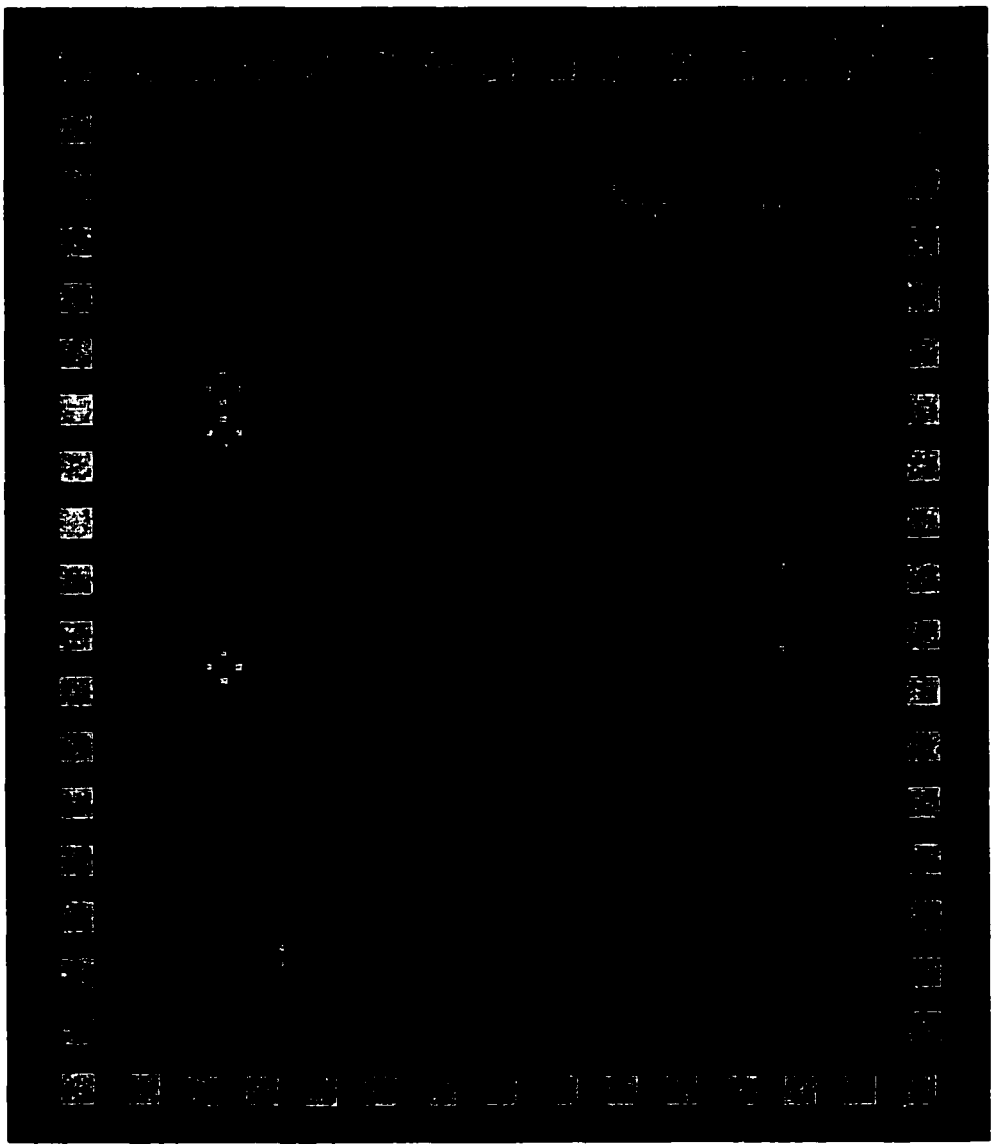


Figure 46 Die photo

6.3 Clock distribution

As we discussed before, 20ps timing error will degrade the performance by 1 bit. Careful clock distribution is required to maintain good performance. The tree structure shown in Figure 47 has been used to maintain nearly the same propagation delay on important clock and timing lines.

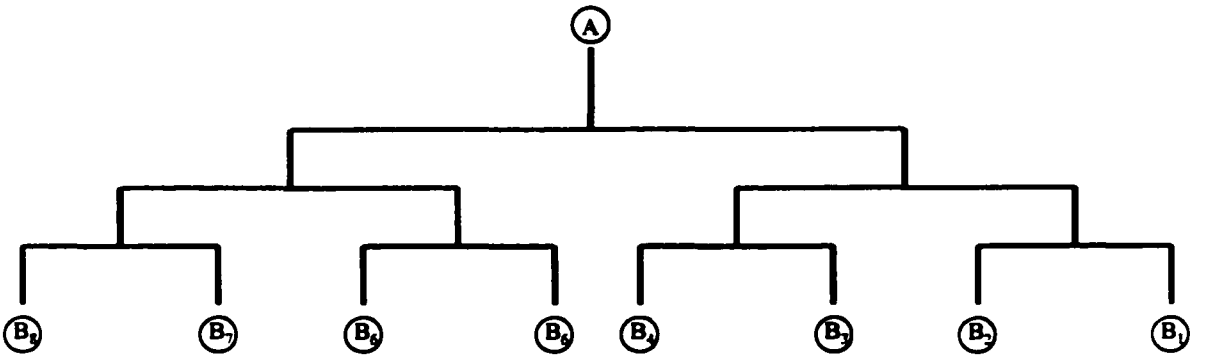


Figure 47 Tree structure

As shown in Figure 47, by using the tree structure, the signal delay from point A to B_i, i=1,2,...,7 can be maintained the same.

6.4 Channel routing

One disadvantage of our proposed architecture was discovered during the layout. Between the comparator array and error correction circuitry, more than 1,500 paths needed to be connected. We refer to this routing as channel routing, which is shown in Figure 48. Since we could not use an auto routing tool like Silicon Ensemble, the channel routing was done manually, which turned out to be very tedious.

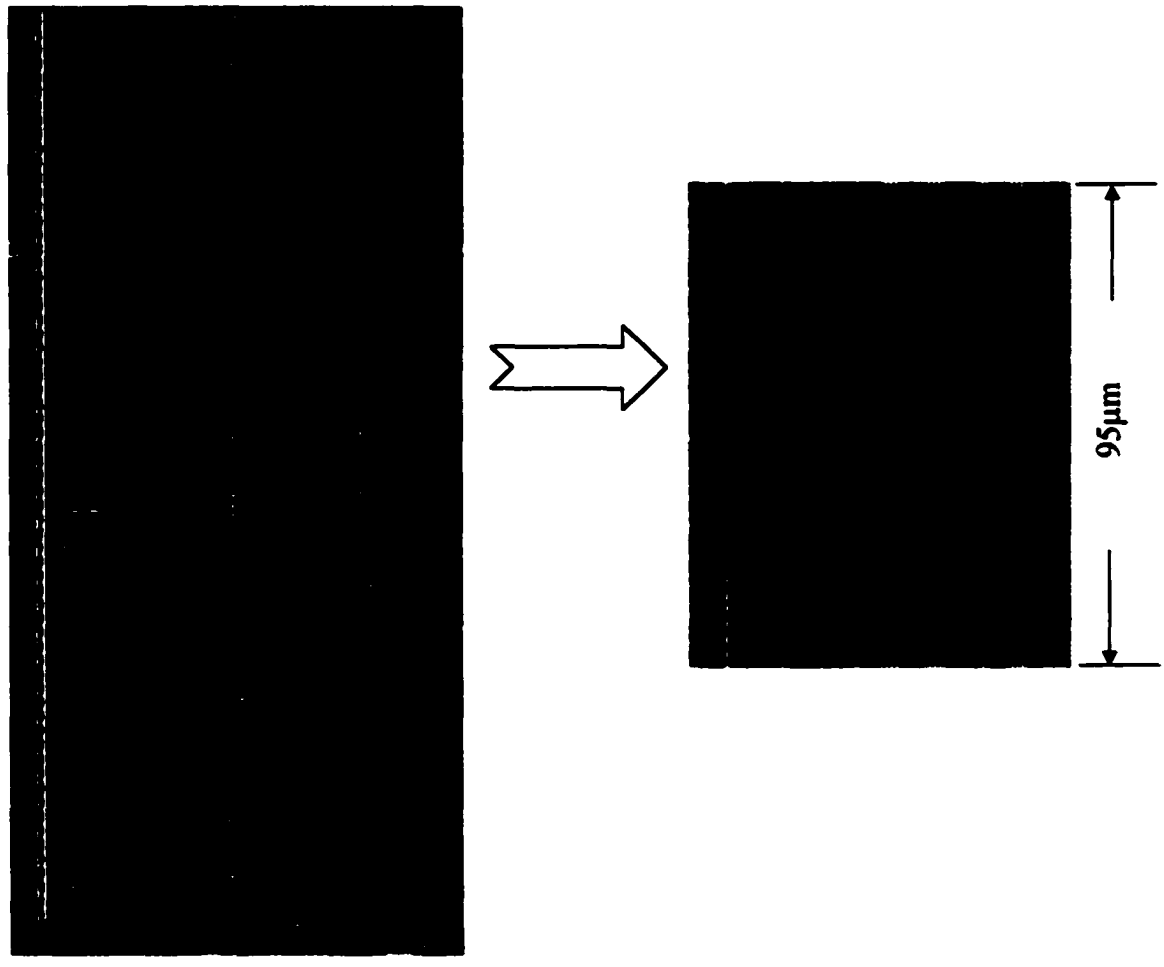


Figure 48 Channel routing

CHAPTER 7 TESTING

Two four layer Printed Circuit Boards (PCB) have been designed using EAGLE™ and fabricated to test this high speed A/D converter. The first board was designed to test the die packaged in a TQFP64 package. From the testing result, it showed that the chip can work up a to 600MHz sampling speed and achieved an SNR higher than 32dB with up to 30MHz analog inputs. Approximately 200mV peak to peak ground bounce was observed on the board. In order to minimize the ground bounce and power supply noise, another four layer PCB was designed to enable chip-on-board testing in which chips were bonded onto the Printed Circuit Boards directly to avoid package leads. This chip and PCB combination achieved a highest acquisition speed of 900MS/s.

7.1 High speed PCB design

7.1.1 Bonding diagram

The bonding diagram of this analog-to-digital converter is shown in Figure 49. In the total of 64 leads, twenty-six are digital outputs. A total of twenty-three leads are tied to power supply, ground and substrate. There are four other leads dedicated to guard ring and shielding. The rest of the leads are for analog inputs and reference bias inputs.

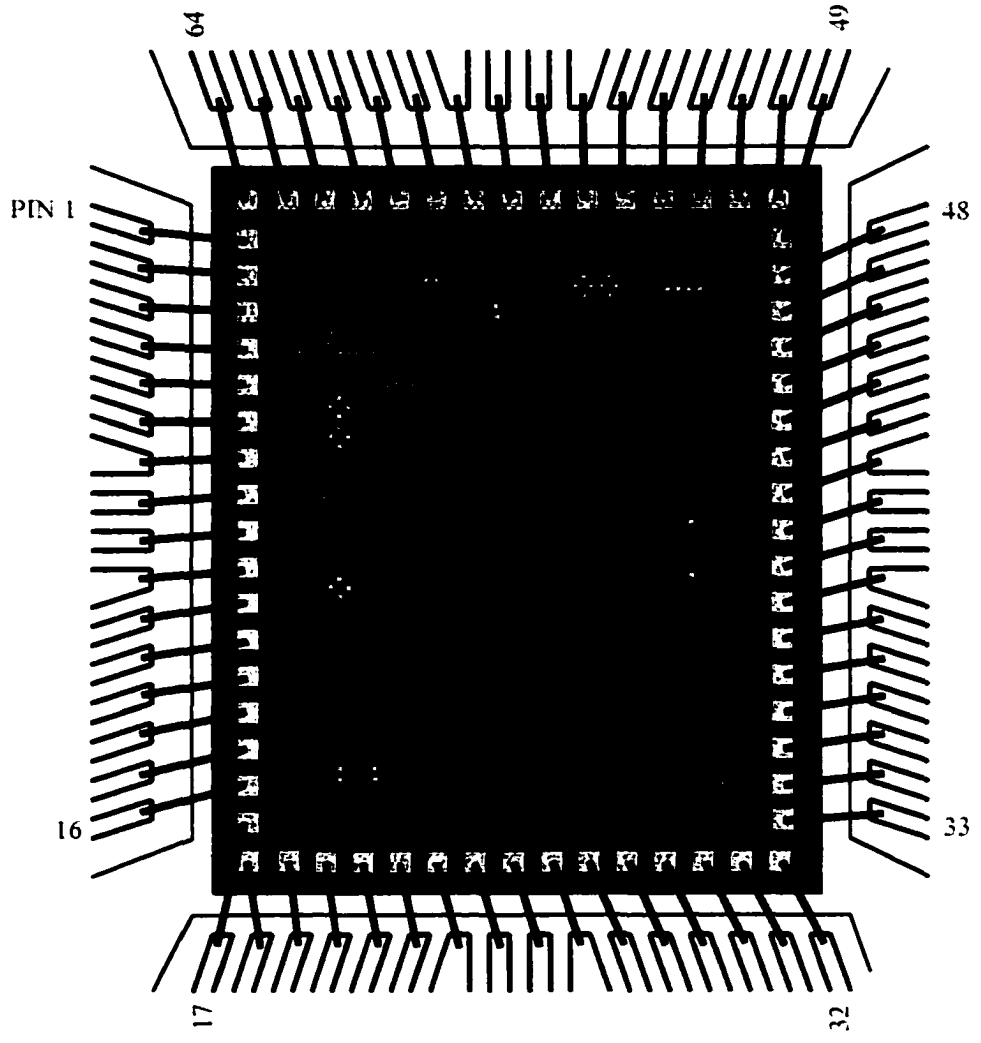


Figure 49 Bonding diagram

7.1.2 Package

A Thin Quad Flat Pack (TQFP) package with 64 leads was initially used which has relatively good high frequency performance. It has relative low parasitic inductance in comparison to PGA and DIP packages. In Table 7, computed lumped element electrical parameters for 10 x 10 x 1 mm 64 lead TQFP package are given [56]. As we can see from

Table 7, for TQFP64 packages, the total parasitic inductance of the leads at the corners are relatively high, such as lead 01 and lead 16. From Table 7, we can observe that the total parasitic inductance for the corner leads is around 4nH, while the total parasitic inductance for the center leads is around 3.2nH.

Table 7 Partial self inductance, bulk capacitance and self resistance

	PACKAGE LEADS			PACKAGE BONDWIRES		
	L(nH)	C(pF)	R(mΩ)	L(nH)	C(pF)	R(mΩ)
Lead 01	1.657	0.366	22.324	2.229	0.180	95.772
Lead 02	1.570	0.397	21.773	2.139	0.184	92.931
Lead 03	1.497	0.384	20.657	2.073	0.177	90.331
Lead 04	1.428	0.373	19.792	2.016	0.172	88.433
Lead 05	1.364	0.364	18.949	1.958	0.167	86.601
Lead 06	1.317	0.358	18.359	1.912	0.163	85.271
Lead 07	1.280	0.353	17.825	1.901	0.162	84.878
Lead 08	1.243	0.361	17.736	1.907	0.166	84.543
Lead 09	1.233	0.360	17.726	1.911	0.166	85.552
Lead 10	1.264	0.353	17.915	1.902	0.163	85.448
Lead 11	1.307	0.355	18.379	1.920	0.163	86.125
Lead 12	1.356	0.364	19.113	1.940	0.167	86.719
Lead 13	1.411	0.372	19.910	1.984	0.171	88.704
Lead 14	1.481	0.383	20.740	2.062	0.178	91.521
Lead 15	1.558	0.395	21.854	2.146	0.184	94.581
Lead 16	1.657	0.368	22.196	2.238	0.181	97.659

7.1.3 High speed four layer board design

High speed PCB design is also important in high speed integrated circuit testing. When signal frequencies go higher than 100MHz, RF effects come into play [57].

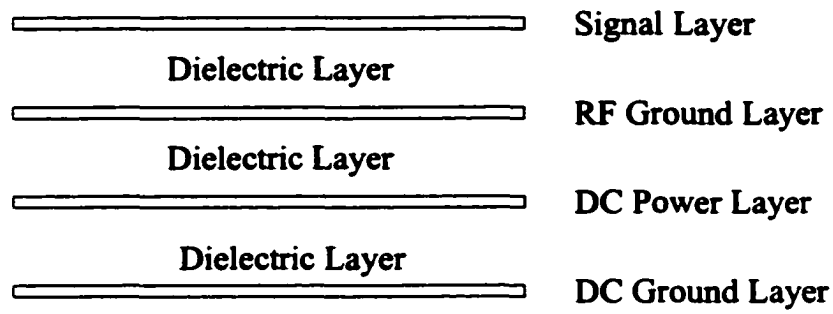


Figure 50 Cross-section of the four layer PCB

Figure 50 shows the cross-section of the four layer PCB. The first layer is the signal layer. The second layer is the RF ground layer in order to have precise impedance control for high speed RF signals on the first signal layer. Since the analog signal and clock signal are running at high frequency (higher than 200MHz), the width of the signal route and the thickness of the dielectric layer between the signal layer and RF ground layer are precisely controlled to ensure matched impedance [58].

Figure 52 shows the first signal layer of the board. The fully differential input signals are generated through a transformer with a center tap. The DC bias of the center tap of the transformer is generated using a reference regulator AD780 from Analog Devices, Inc. Four channels, totaling 24 bits along with two trigger clocks are brought out from the chip and connected to a high speed TLA 711 Logic Analyzer from Tektronix. Figure 52 shows the photograph of the PCB.

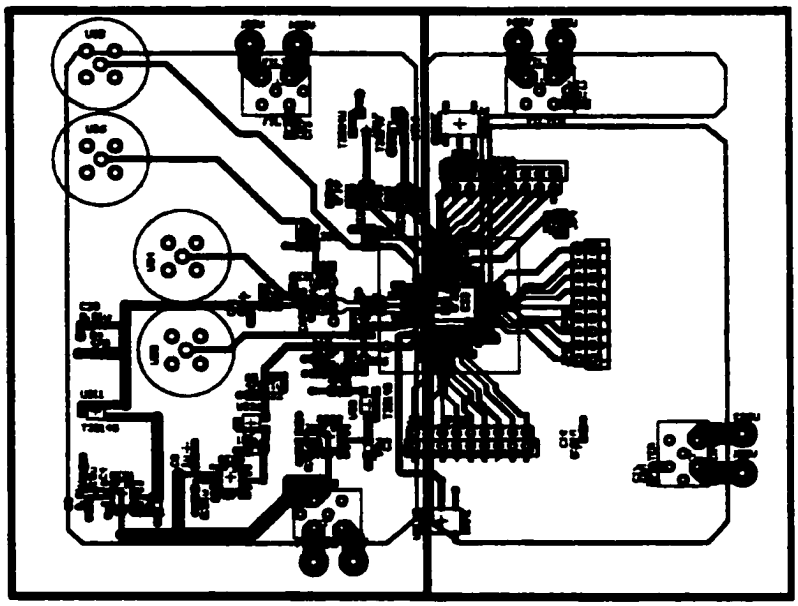


Figure 51 First signal layer of the board

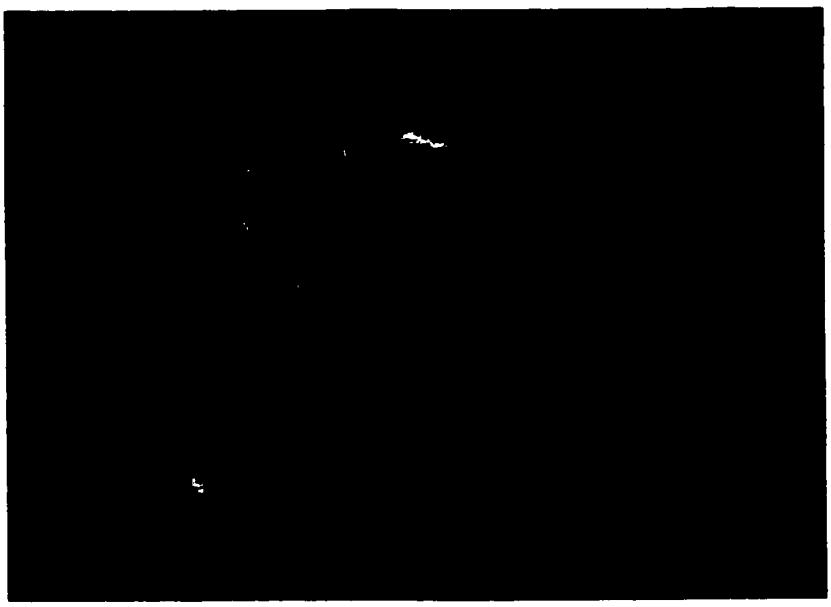


Figure 52 Photography of the board

7.1.4 Testing Setup

Figure 53 shows the testing setup. Twenty-four digital outputs are collected using a high speed TLA 711 Logic Analyzer. By performing an FFT on the analyzer outputs, we have determined the dynamic performance of the chip, including SNDR and ENOB.

7.1.5 Testing results

As we previously mentioned, four channels, totaling 24 bits are brought out from the chip and collected by the high speed logic analyzer. The logic analyzer permits a high speed sampling function at 2Gsample/s. Figure 54 shows the output of the trigger clock signal and the four combined outputs. As we can see, the four channels are synchronized by the internal clock. The glitches are caused by improperly sampling because the analyzer timing is not synchronized with the A/D converter. By properly establishing the trigger point, the four channels of digital outputs can be obtained, which is shown in Figure 55

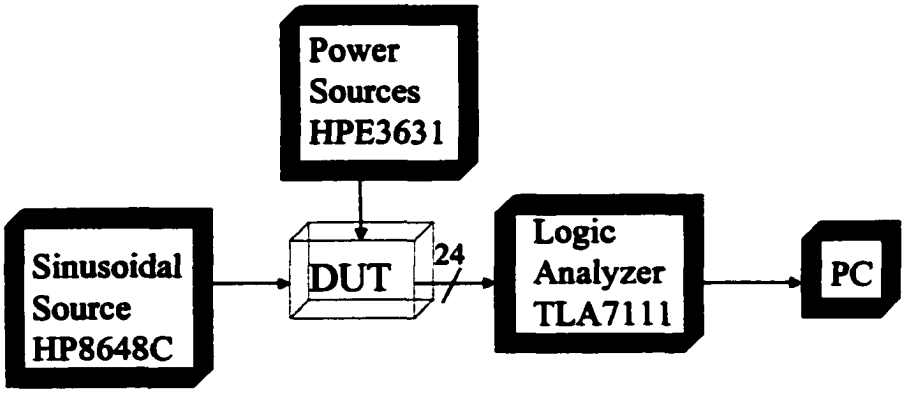


Figure 53 Testing setup

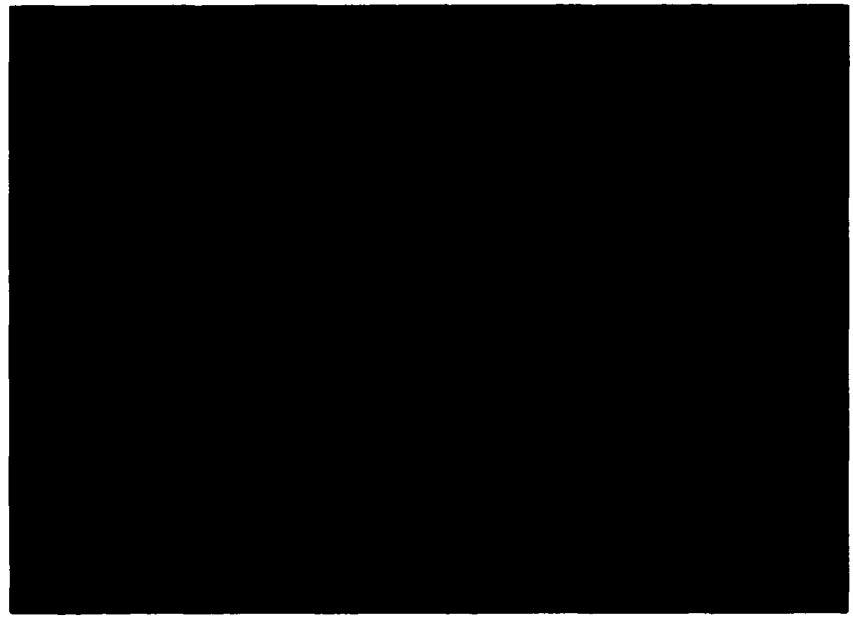


Figure 54 Trigger clock and synchronous four channels output at f_s = 600MHz and f_{in} = 34.1MHz

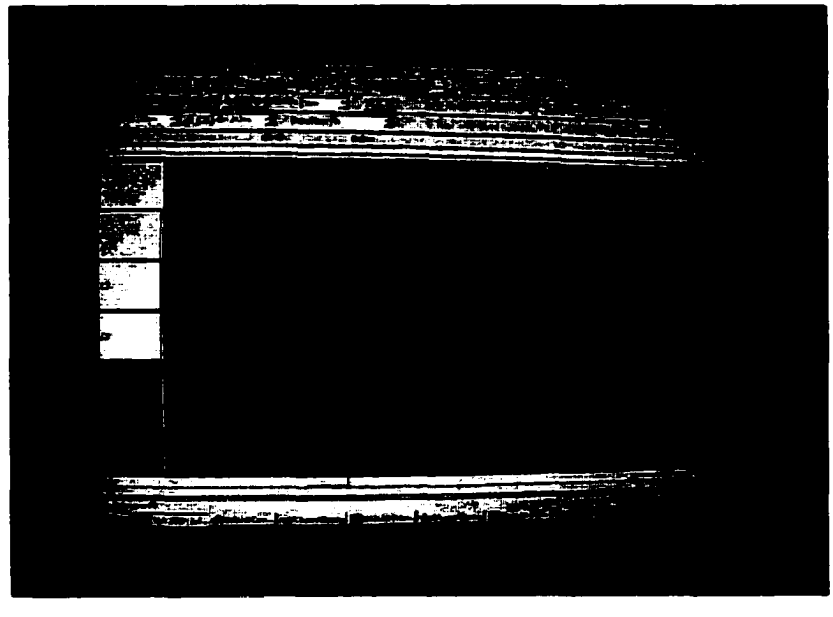


Figure 55 Four channel digital output with proper timing synchronization

Based on the timing and digital outputs, the correct trigger points can be set for the four individual channels. Then, the digital outputs can be collected only at the proper trigger points. Figure 55 shows this digital output. Then, the data can be exported and analyzed through the PC. The chip has been tested at 600MHz sampling frequency. For each test, 4096 points were collected using the TLA 711 Logic Analyzer. The data were exported to a PC for FFT. In order to minimize the "leakage" due to FFT, a window function called Black-hamming window was applied before FFT. Then, the SNDR and ENOB can be determined. Figure 56 shows the SNDR vs. analog input frequency when fs = 600MHz.

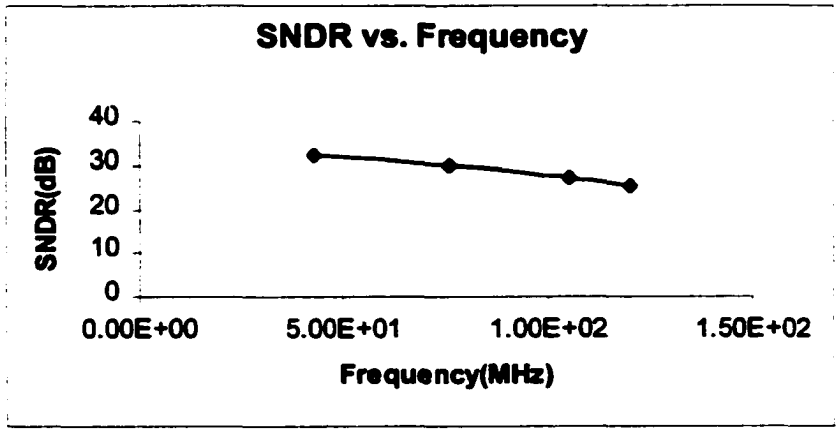


Figure 56 SNDR vs. Frequency at fs = 600MHz

From the testing results, we observe that the ENOB of each channel is only a little smaller than that of the combined data. This implies that the converter offset mismatch, gain error mismatch and clock skew only contribute a small amount of extra error into the system. However, we observed that ground bounce of 200mv peak to peak exists on the Printed Circuit Board. In order to minimize the ground bounce and power supply noise, we turned to

a chip-on-board testing architecture. In this architecture, the raw dies are directly assembled on the Printed Circuit Board (PCB) without using any package. By doing this, the parasitic inductance due to package leads can be eliminated. Also, the wire bonds can be shortened by arranging the PCB bonding pads closer to the die. All these help to minimize the parasitic inductance dramatically. In order to minimize ground bounce of analog circuitry and substrate noise, the analog ground pins and substrate pins are down-bonded directly to the ground plane. This will cut the wire bond inductance to an even smaller value.

7.2 Prototype of the second PCB

7.2.1 PCB design

The second high speed PCB design follows the same theory of the first PCB design. It is a four layer board with a size of 4.5" x 5". The bonding pads on the board are properly placed, so the die can be bonded directly onto the board. All the bonding pads on the board are placed as close to the die as possible to minimize the bonding wire.

Figure 57 shows one of the four layer PCBs for chip-on-board testing. The testing chips were bonded directly onto the PCBs by Polarfab Inc. By doing chip-on-board testing, the chip achieved a highest functional acquisition speed of 900MS/s. Figure 58 shows the synchronous four channels output with sampling frequency at 900MHz and analog input at 1.1MHz. As we can observe from Figure 58, the combined output of each channel gives a good sine wave output even at 900MS/s.

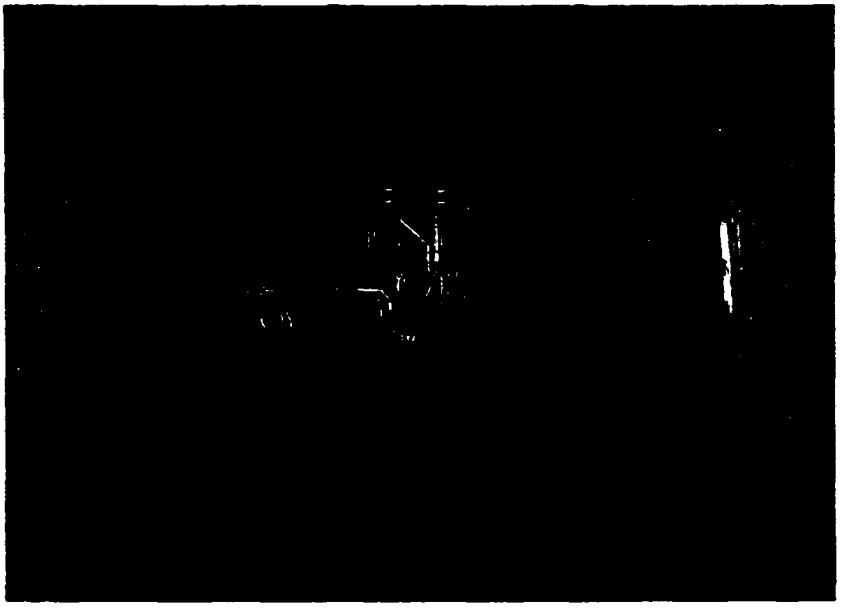


Figure 57 4 layer PC board for chip-on-board testing. Board size is 4.5" x 5"

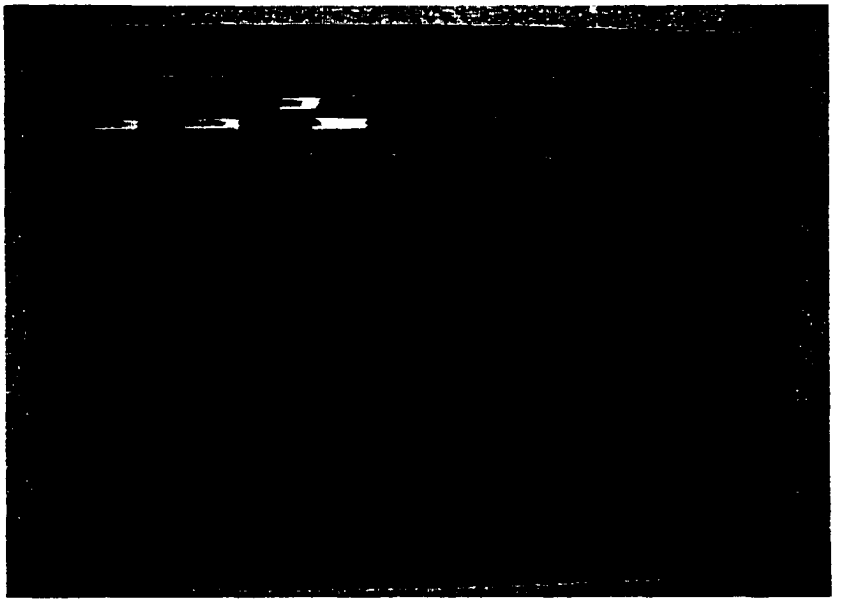


Figure 58 Synchronous four channels output at f_s=900MHz and f_{in}=1.1MHz

7.2.2 Testing results

Figure 59 shows the FFT results of the combined four-channel digital output at an analog input frequency of 11.7MHz with sampling frequency of 600MS/s. The signal peaks observed at 88.5MHz and 105.3MHz are introduced by local radio station. The measured SNDR is 33.2dB, which implies the ENOB is equal to 5.22 bits. From Figure 59, we can't observe any tones due to mismatch between the channels in terms of gain, converter offset and timing skew, which implies that the individual ADCs are inherently almost identical in terms of gain and converter offset. However, at higher frequency, due to timing skew, the composite ADC performance is degraded by the timing skew between the channels. The performance comparison of the composite ADC and the average of four individual ADCs at a sampling frequency of 600MS/s is shown in Figure 60. As we can see, at low frequency, the timing skew doesn't degrade the performance of the composite ADC. However, the performance of the composite ADC rolls off compared with the average SNDR of four individual ADCs. As we discussed before, the signal-to-noise ratio due to timing skew is a function of $\sigma_t f_{in} / f_s$. As the analog input frequency f_{in} increases, the noise contributed to the system due to timing skew will increase. With sampling at 600MS/s, SNDR of the composite ADC is about 2dB less than that of the average of four individual ADCs at an analog input frequency of ¼ of sampling frequency. Overall, the mismatch between channels only degrades the performance a little, which implies that the technique that we demonstrated here to minimize the mismatch between the channels in terms of gain, converter offset and timing skew is effective. Figure 60 shows the measured SNDR of the converter as a function

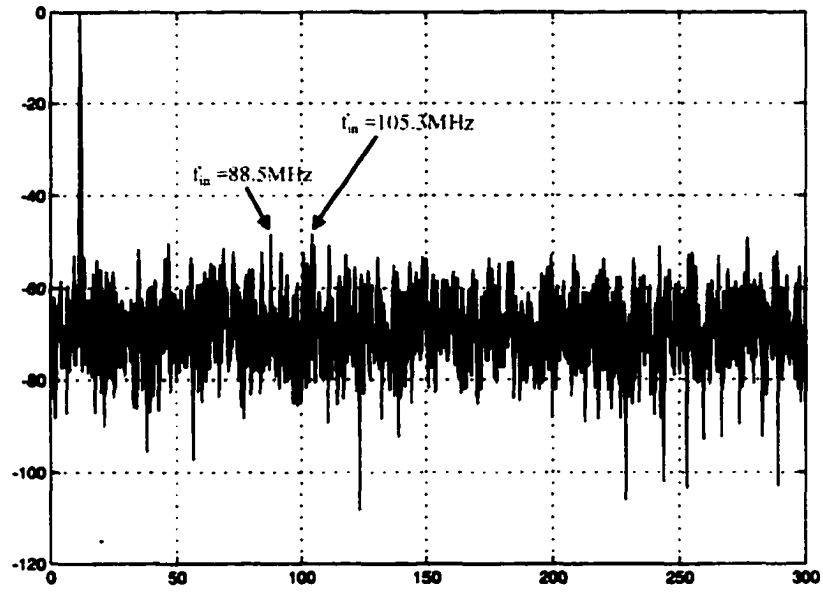


Figure 59 FFT at fin=11.7MHz when sampling at 600MS/s

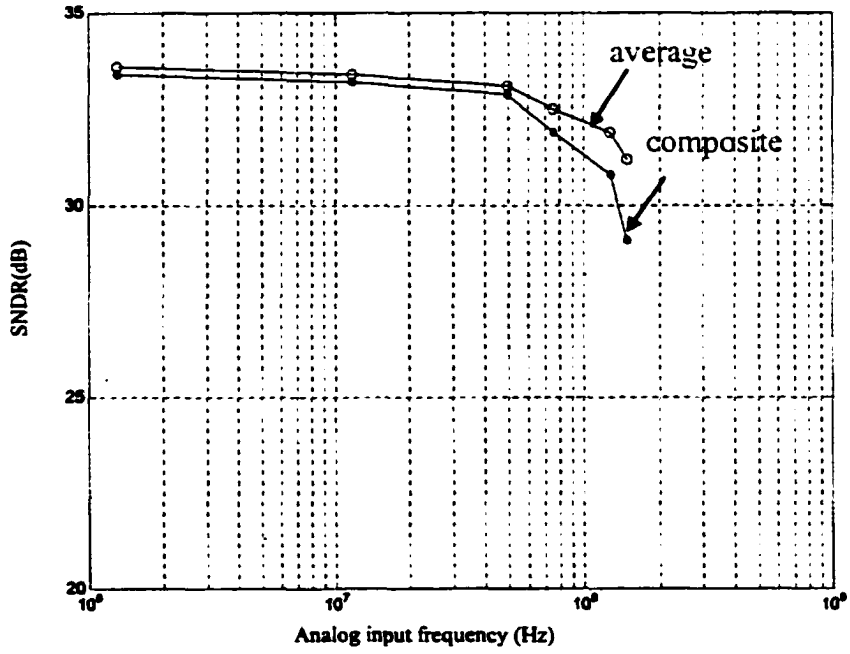


Figure 60 Performance comparison between composite ADC and average of four individual ADCs with sampling frequency of 600MS/s

of the input frequency at a sampling frequency of 600MHz. The SNDR of the converter is higher than 29dB with input frequencies up to 150MHz

Figure 61 shows the performance comparison between the two different boards. The sampling frequency for both tests is 600MHz. As we can see, chip-on-board testing really makes a difference in the high frequency range. About 1b improvement is achieved at an input frequency of 150MHz. There are two reasons for this improvement of the ADC performance.

1) Chip-on-board testing allows the dies to be bonded directly onto the Printed Circuit Board. As shown in Table 7, the parasitic inductance due to package leads is about the same as that of the bonding wire for package type TQFP64. By doing chip-on-board testing, the package leads have been eliminated, which implies that the total parasitic inductance has been reduced to half of the original size. Also, the bonding wires are

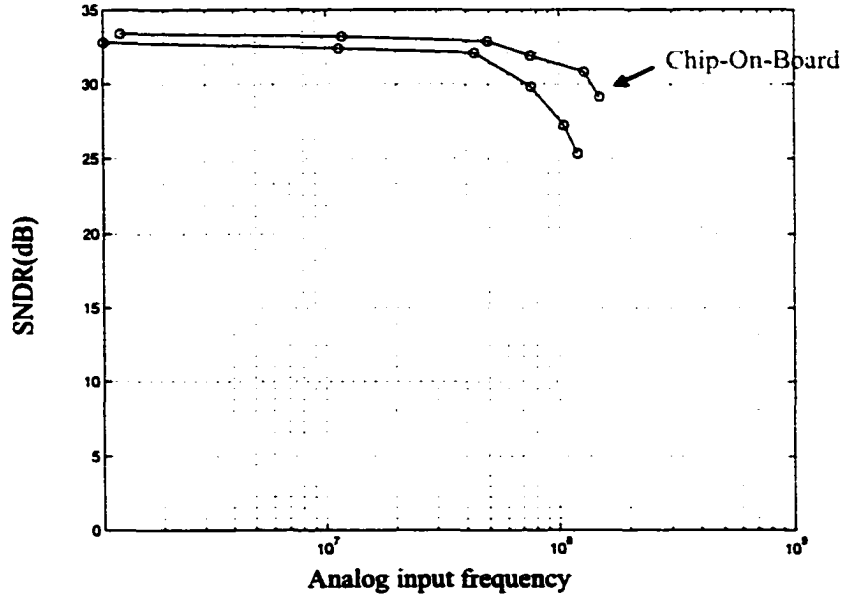


Figure 61 Performance comparison between two different board methods

shorter than that with package. In conclusion, for chip-on-board, less parasitic inductance appears at the I/O pins.

2) The digital ground plane and analog ground plane are connected through ferrite bead on the Printed Circuit Board instead of having one big plane for digital ground and analog ground. In this specific design, the digital ground bounce was much higher than the analog ground bounce. By having one big ground plane for both digital ground and analog ground, the digital noise will interfere with the analog circuitry through the ground plane, which degrades the performance.

Due to both efforts on the second testing board, the ground bounce is much less than before. About 80mV ground bounce was observed at the analog supply of the second board, compared with 200mV peak to peak ground bounce that was observed with the first testing board.

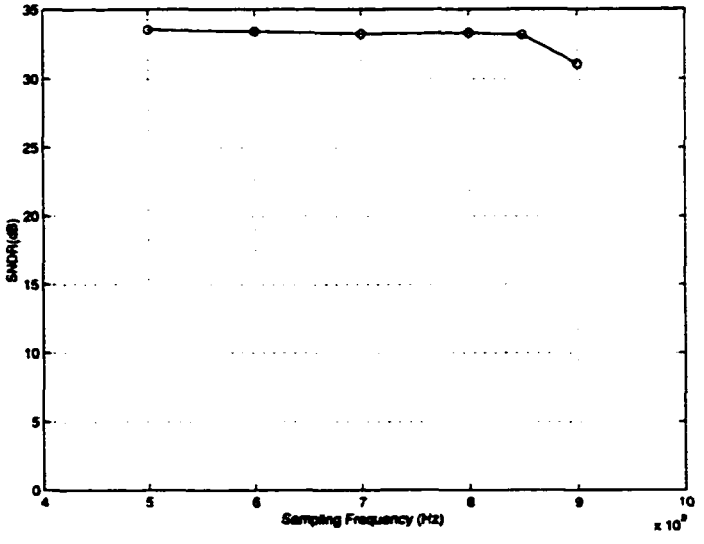


Figure 62 SNDR vs. Sampling frequency at input frequency of 1.1MHz

Figure 62 shows the measured signal to noise and distortion ratio (SNDR) of the converter as a function of the sampling frequency with a fixed input frequency at 1.1MHz. As we can see from Figure 62, SNDR of the converter stays flat and starts to roll off at a sampling frequency of 880MHz. The converter achieves higher than 31dB performance even at a sampling frequency of 900MHz.

The chips have been tested to higher than 400MHz analog input frequencies at 900MHz sampling frequency. Figure 63 shows SFDR as a function of input frequency. From Figure 63, we can see that SFDR is higher than 30dB even with input frequency higher than 400MHz at 900MS/s.

One comparison with previous work is shown in Figure 64. Our work achieves higher signal to noise and distortion ratio at much higher analog input frequency at sampling frequency of 900MS/s.

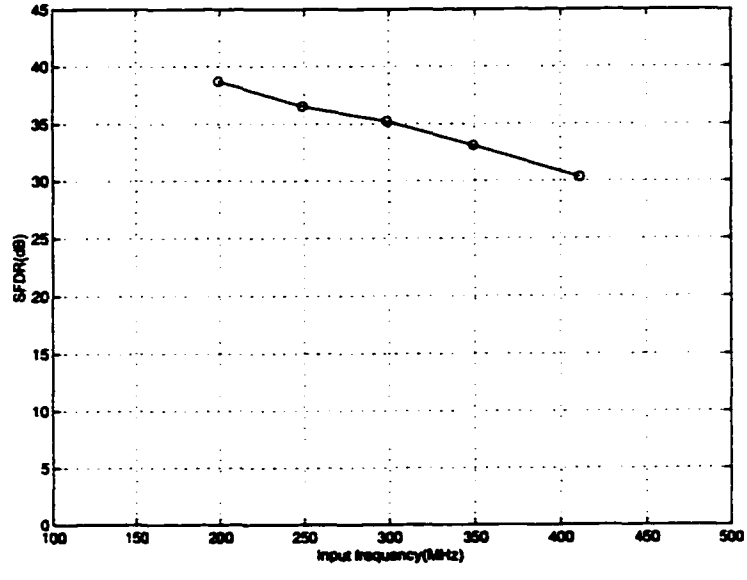


Figure 63 Measured SFDR as a function of input frequency at 900MS/s

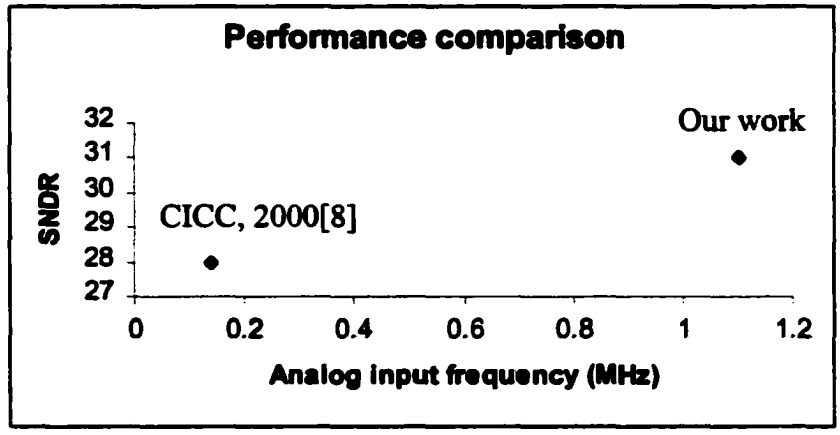


Figure 64 Performance comparison at sampling frequency of 900MS/s

Table 8 Experimental summary

Resolution	6b
Maximum Acquisition Speed	900MHz
Active area	2.08mm^2
SNDR Fin=1.1MHz, fs=900MHz	31dB
SNDR Fin=150MHz, fs=600MHz	29dB
Power dissipation fs=600MHz	250mW Analog part (150mW) Digital part (100mW)
Power dissipation fs=900MHz	450mW Analog part (200mW) Digital part (250mW)
Power supply	2.5volts
Technology	0.25μ CMOS technology

7.3 Future work

The time-interleaved architecture can achieve even higher conversion speed if we can find a better way to generate multi-phase clocks. PLL or DLL should be a more efficient way to do this if phase jitter and phase skew can be minimized. My colleague Lin Wu did a lot of research on this and achieved great results[59]. The future work would be to combine her clock generator technique with the time-interleaved ADC architecture and achieve higher than 1GS/s ADCs.

CHAPTER 8 PROPERTIES OF THE VCR

As we mentioned before, high linearity and high resolution A/D and D/A converters are demanded for measurement equipment, digital video systems and digital audio applications. Starting from this chapter, a novel and highly linear device --- voltage controlled resistor (VCR) will be introduced and analyzed. The calibration principles of the VCR for matched current sources are demonstrated. Due to the high trimming resolution, high precision digital-to-analog converters can be designed based on this technique.

8.1 Structure of the VCR

Figure 65 shows the structure of the VCR. It is designed to be fabricated in conventional n-well CMOS technology. The device appears similar to a MOSFET, however the poly or metal gate is over field oxide instead of thin oxide. The mechanism whereby the resistivity is modulated by the gate voltage is the variation in the well surface electron concentration with applied bias. For example, a positive gate bias which increases the electron concentration near the surface will decrease the resistance of the VCR (if it is fabricated in an n-well process).

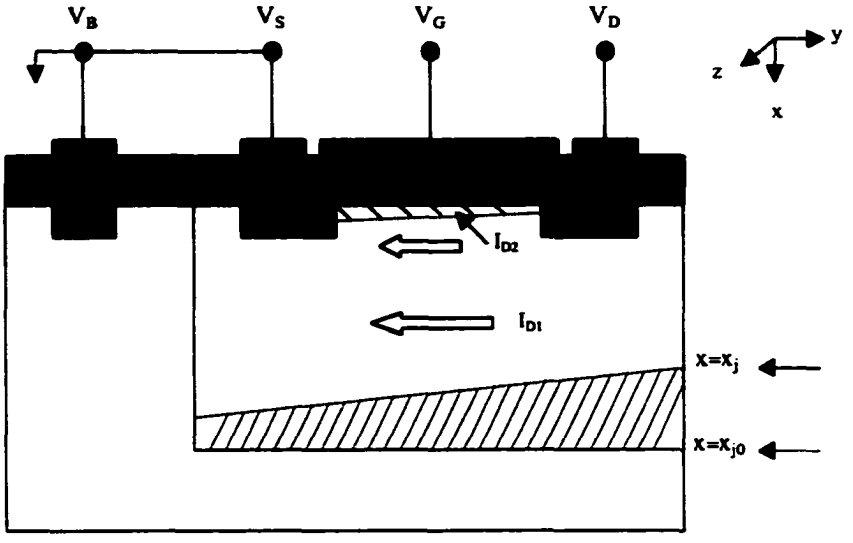


Figure 65 Cross Section of VCR

8.2 Characteristics of the VCR

The finite element device simulation software ATLAS™ was used to simulate the characteristics of this device and to confirm the assumptions. The simulated cross-section of the n-well electron concentration distribution for a two- gate VCR structure is shown in Figure 66. The interface between oxide and substrate is at y=0 and the thickness of the field oxide is about 1μm. Each of the two gates is 4μm wide. From the scale of Figure 66, it can be seen that gate 1 goes from x=5μm to x=9μm and gate 2 goes from x=11μm to x=15μm. The spacing between gates is 2μm and five volts is applied to both gates. The lateral voltage drop between terminal D and S is 1 volt. In order to observe the adjustment of electron concentration underneath the gates more clearly, Figure 67 show a close-up of the region between the gates.

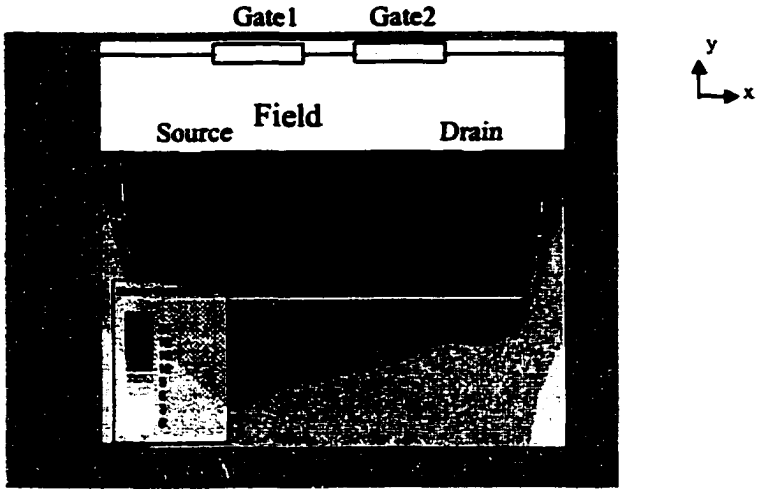


Figure 66 Electron Concentration distribution from ATLAS™

From Figure 67, we can easily see that with a bias voltage of 5 volts applied to the gates, the electrons are attracted to the surface of the n-well. However the surface electron concentration around 10 μm (x-direction) in this picture is not changed. The reason for this is that there is no gate overlay on the top of the field oxide from x=9μm to x=11μm, and

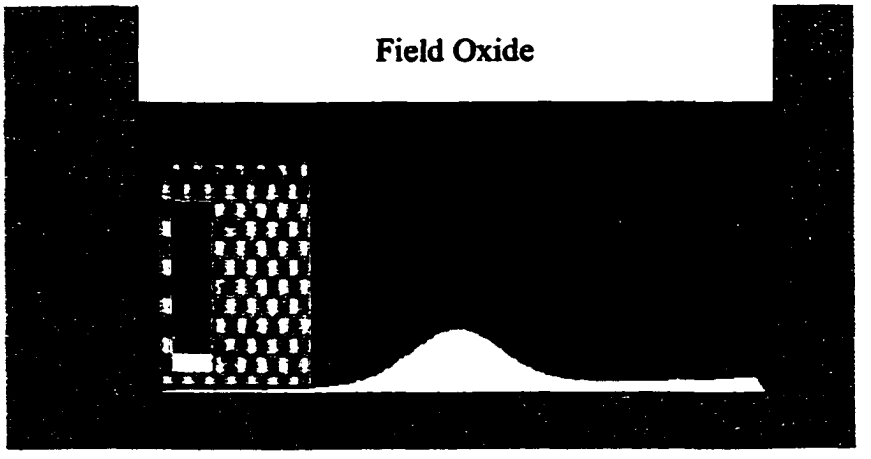


Figure 67 Electron distribution between the gates in the n-well

hence no vertical electrical field exists there to attract electrons to the surface.

A single gate VCR structure with a metal field overlay layer was fabricated in a 2 μm n-well CMOS process (via MOSIS) and evaluated at different bias and temperature conditions using an HP4145A parameter analyzer and a temperature controlled oven with packaged parts. The following table shows the measured results.

Table 9 The resistance of VCR and change in resistance at different temperatures (MOSIS 2μ technology)

T(°C)	R (kΩ) at V_{GS} = 0V	R (kΩ) at V_{GS} = 5V	ΔR/R (%)
0.0	6.53	6.28	3.83
9.7	6.98	6.70	4.01
19.9	7.45	7.16	3.89
24.7	7.69	7.38	4.03
29.9	7.94	7.62	4.03
35.1	8.21	7.88	4.02
39.9	8.46	8.12	4.02
50.2	9.02	8.64	4.21
60.3	9.60	9.20	4.17

Table 10 The resistance of VCR and change in resistance at different temperatures (TSMC 0.25μ technology)

T (°C)	R(kΩ) Vgs=0V	R(kΩ) Vgs=5V	ΔR/R (%)
0	2.1840	2.1243	2.812
20	2.3073	2.2448	2.784
40	2.4653	2.3988	2.771
60	2.6338	2.5652	2.674
80	2.8173	2.7418	2.754
100	3.0470	2.9656	2.745
120	3.2341	3.1478	2.742
140	3.4473	3.3550	2.751

From Table 9, about a 4% resistance change was observed with gate bias voltage changing from 0V to 5V. The measured change in resistance due to gate biasing only depended weakly upon temperature.

Another set of devices was fabricated using TSMC 0.25μ CMOS technology. The test structure are VCRs of L=24um (y direction) and W=12um (z direction) with 80um spacing between in the z direction (Figure 65). It was measured using an HP4155A Semiconductor Parameter Analyzer. About 2.8% resistance change was observed with gate bias changing from 0V to 5V as shown in Table 10. This data also shows that the measured change in resistance due to gate biasing only depended weakly upon temperature.

8.3 Proposed models for VCR

8.3.1. DC model

A 4-terminal model and a 3-terminal model for diffused resistors were previously proposed [60]-[64]. A simplified DC model has been derived for this 4-terminal Voltage Controlled Resistor. With voltage drop along drain and source, the drain current is the summation of I_{D1}(current in n-well) and I_{D2}(current due to electron accumulation close to the well surface). I_{D1} is given by (Appendix B)

$$I_{D1} = \frac{q\mu\mu_{w} V_{DS} W_{eff}}{L_{eff}} x_{jeff} \qquad (72)$$

where μ is the electron mobility in n-well, N_w is the electron concentration in n-well, and V_{DS} is the voltage drop across drain and source. W_{eff} and L_{eff} are the effective width and length of the channel in the n-well region and x_{jeff} is the effective depth of the n-well.

$$x_{jeff} = x_{j0} - \frac{2}{3}\alpha\left(V_{DS}^{\frac{1}{2}} + \frac{3}{2}\varphi V_{DS}^{-\frac{1}{2}} + \frac{3}{4}\varphi V_{DS}^{-\frac{3}{2}}\right) \qquad (73)$$

x_{j0} is the metallurgical junction depth. ϕ is the build-in voltage and α is the depletion width factor, which can be derived using the following equation.

$$\alpha = \sqrt{\frac{2\varepsilon N_{sub}}{qN_w(N_w + N_{sub})}} \qquad (74)$$

$$\varphi = \frac{kT}{q}\ln\left(\frac{N_w N_{sub}}{n_i^2}\right) \qquad (75)$$

N_W is the doping concentration in the n-well and N_{sub} is the doping concentration in the substrate. The drain current due to electron accumulation close to the n-well surface can be calculated using the following equation.

$$\begin{aligned} I_{D2} &= 0 && V_{GS} = 0 \\ I_{D2} &= \frac{2\mu' C_{ox} W_{eff}}{L_{eff}}\left(V_{GS} - \frac{1}{2}V_{DS}\right)V_{DS} && V_{GS} > 0 \end{aligned} \qquad (76)$$

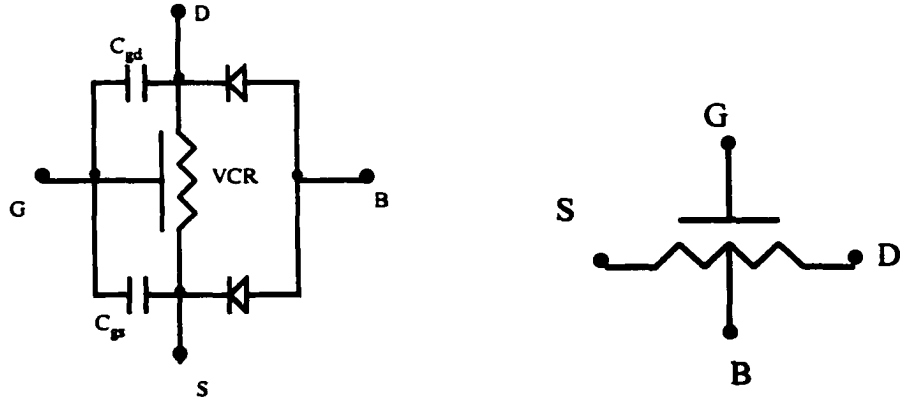
where μ' is the electron mobility in the accumulation channel which is a function of electron concentration. The total drain current is

$$I_D = I_{D1} + I_{D2} \qquad (77)$$

8.3.2 Macro model

A SPICE macro-model of this device has been developed based upon the equation above with various parasitic elements as shown in Figure 68 (a). The device is shown symbolically in Figure 68 (b).

Figure 69 shows the relation between Ids and Vgs of the VCR (fabricated in TSMC 0.25 μ technology) at Vds equal to 2 volts. The curve fit DC model of equation (77) matches the testing result to a maximum deviation of 0.03%. From this figure, we can see that I_D has a nearly linear relation with Vds. About 2.8% resistance change was observed with gate bias changing from 0v to 5v. Due to the gate overlay being on the top of the field oxide, C_{ox} is much smaller than that of a thin oxide MOSFET. By adjusting the bias voltage on the gate, we have fine control of the resistance of the n-well resistor.



(a) Macro-model of the device (b) Symbol of the device

Figure 68 VCR models

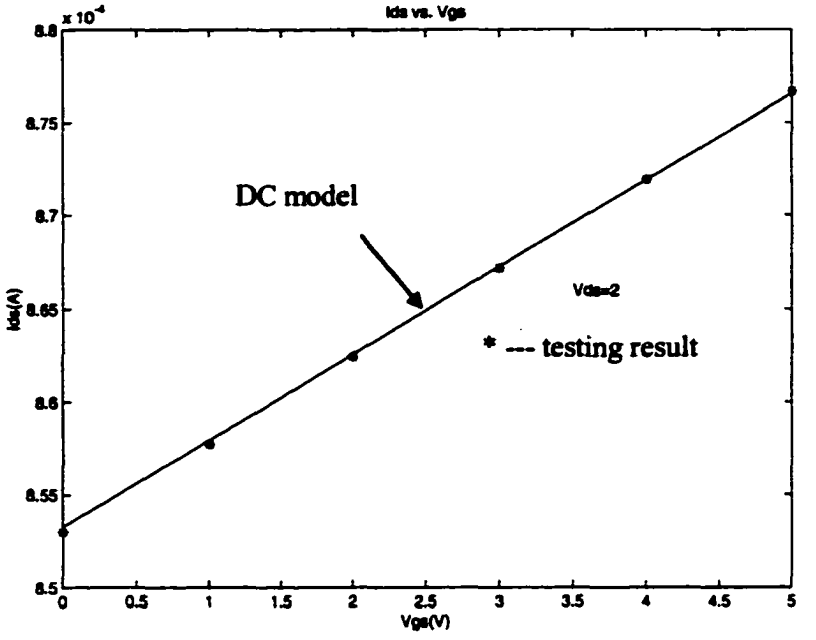


Figure 69 I_{DS} versus V_{GS}

CHAPTER 9 CALIBRATION PRINCIPLES WITH VCR FOR MATCHED CURRENT SOURCES

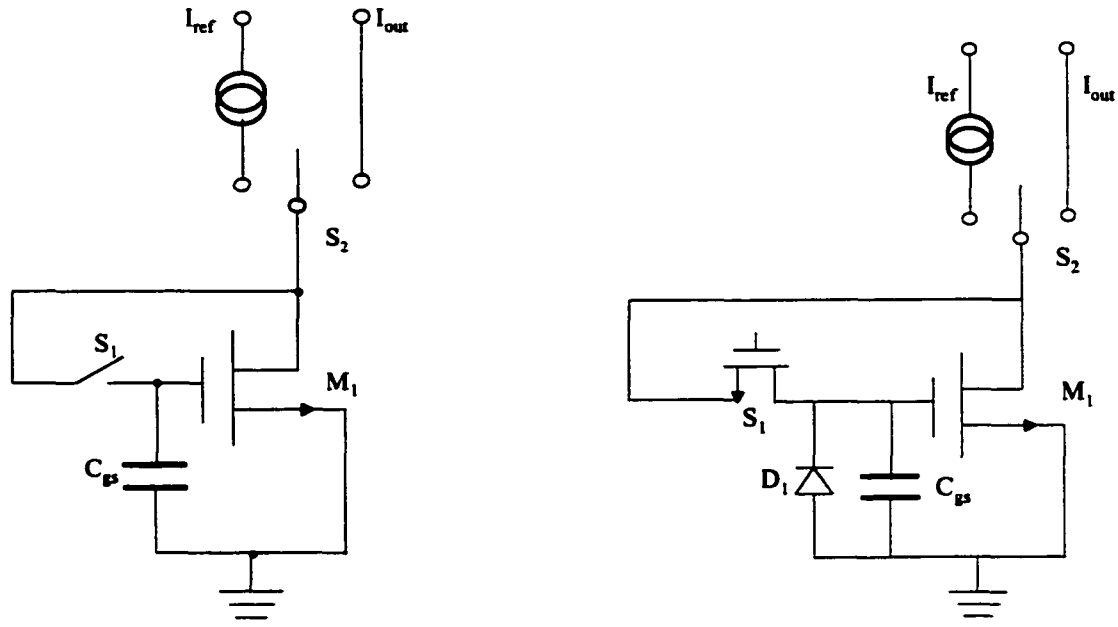
9.1 Current calibration principle

A favorable way to achieve matching currents is dynamic element matching. The basic idea is to dynamically adjust components (typically current sources) in order to make them match [28]. Figure 70(a) shows the basic operation of the system, which has calibration mode and operational mode.

In the calibration mode, switch S_1 is closed and S_2 is switched to I_{ref}. During this time period, the gate voltage V_{gs} of M_1 is calibrated. Then, in the operational mode, S_1 turns off, and S_2 switches to the current output. In an ideal scenario, the gate voltage V_{gs} of M_1 will not change because the charge is stored on the gate capacitance C_{gs}. Provided that V_{ds} of M_1 is the same, I_{out} is expected to be the same as I_{ref}. In reality, however, there are two major error sources.

9.2 Calibration principles with VCR for matched current sources

Figure 70(a) shows the basic operation of the system. It has calibration mode and operational mode. In the calibration mode, switch S_1 is closed and S_2 is switched to I_{ref}.



(a) Ideal scheme (b) Real scheme

Figure 70 Dynamic calibration

Figure 70 (b) shows the real calibration circuit. One error comes from switch S_1, which is implemented by MOSFET. When the operation of the system transition from calibration mode to operational mode, S_1 turns off, its channel charge q_{ch} is partially dumped onto C_{gs}. The changes in charge on C_{gs} implies the voltage change of V_{gs}. Based on the characteristic of MOSFET, I_{out} will differ from I_{ref} [65].

$$I_{out} = I_{ref} - \frac{3}{2}\sqrt{\frac{2\mu}{C_{ox}}} * \frac{q_{ch}}{L}\sqrt{\frac{I_{ds}}{WL}} \qquad (78)$$

where μ is electron mobility, C_{ox} is oxide capacitance density, W , L are channel width and length of M_1 respectively.

In equation (78), the second term on the left is the error term introduced by charge injection when S_1 turns off. Another error source is reversed-biased diode D_1, which is the diode between source and substrate of M_1. Even though it is reverse biased, the leakage current will discharge C_{gs}, which implies that the gate voltage will droop. This will also cause I_{out} to differ from I_{ref}. The time dependent drain current due to the diode leakage is [65]

$$I_{ds,leak}(t) = I_{ref} - \frac{3}{2}\sqrt{\frac{2\mu}{C_{ox}}}\frac{1}{L}\sqrt{\frac{I_{ds}}{WL}}I_{leak}t \qquad (79)$$

where

I_{leak} is the leakage current of diode D_1

In equation (79), the second term on the left is the error term caused by the leakage of D_1. Equation (79) implies that after a certain time, the current cell needs to be calibrated again to keep I_{out} in a certain range of I_{ref}. From both equations, we can see that in order to keep the error small, channel width and length of MOSFET M_1 needs to be large, especially the channel length.

Figure 71 shows the scheme of a calibrated current source circuit which has been simulated using HSPICE™ [66]. It is a dynamic element matching circuit which can produce multiple output currents that are very closely matched. The MOS transistors M0, M1, M3 and VCR1 form the reference current.

Output currents I_1 and I_2 will be alternately switched to M_2 in order to be calibrated. During the calibration cycle, the voltage at the gate of the VCR is adjusted by a high gain negative feedback such that the voltage at node A is equal to the voltage at node B. After

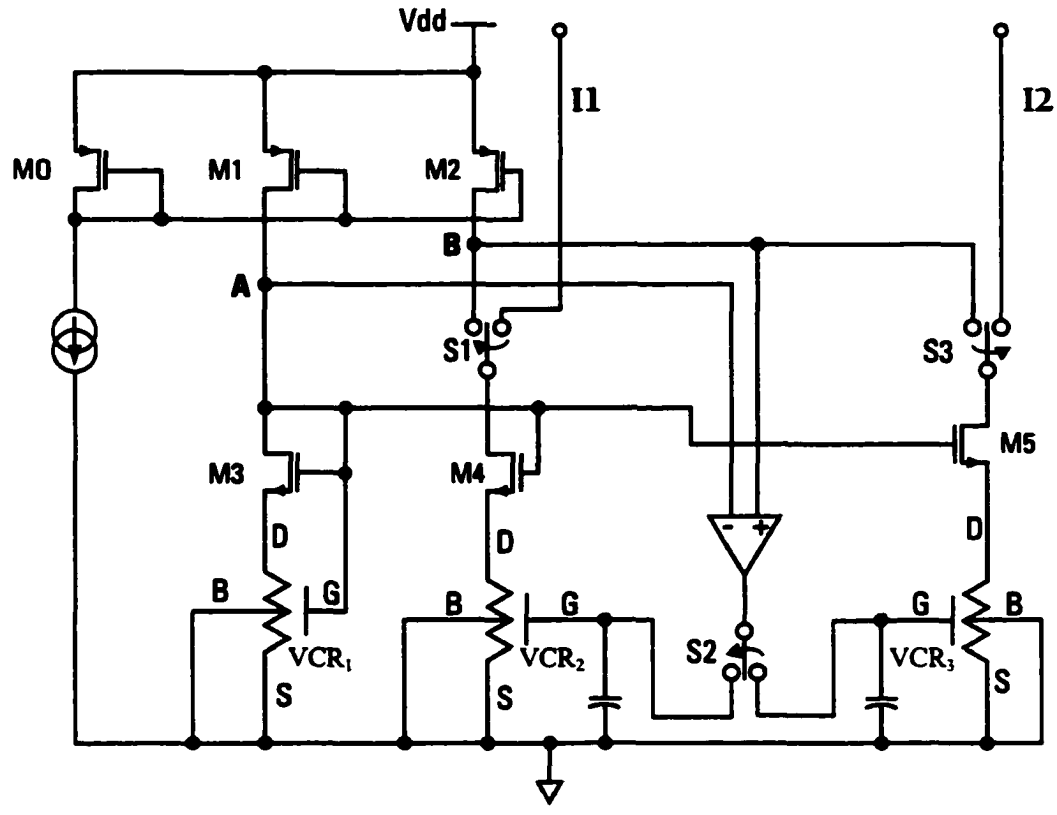


Figure 71 Calibrated current source circuit

calibration, the output currents are switched to V_{dd} through an output resistor. A macro-model is used for the VCR during simulations. In order to simplify the simulation, based on equation (77), the relation between the resistance of VCR and bias voltage on the gate is assumed to be linear. Figure 72 shows the simulation results using Analog Artist™. The drain currents of M_4 and M_5 are plotted in the figure along with the calibration clocks. In order to demonstrate the ability of calibration, the resistance of the three VCRs were set with 4% deviation to mimic the mismatch between VCRs due to process variations. Despite these mismatches, the currents can be calibrated to 0.01% precision. Because of the trimming capability of the VCR, the mismatch between MOSFETs can also be compensated, high precision D/A converters can be designed based on this high trimming resolution technique.

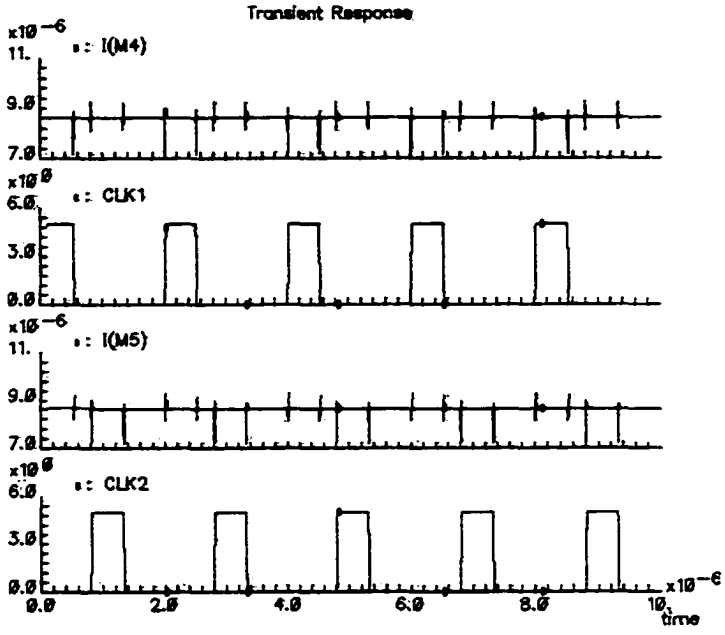


Figure 72 HSPICE™ simulation results

CHAPTER 10 CONCLUSION

In the first part of this dissertation, a four way time-interleaved flash A/D converter is demonstrated using 2.5V digital 0.25 micron TSMC technology. The four on-chip ADCs share a common reference string and preamplifiers to minimize the mismatch between channels. By using two stage preamplifiers, the unity gain bandwidth has been maximized. Based on simulations, the overall unit gain bandwidth of the preamplifier is 6.7GHz and the DC gain of the preamplifier is around 5. Since four ADCs share the same preamplifier, any mismatch in terms of converter offset and gain mismatch will be decreased by the DC gain of the preamplifier. By doing this, nearly the same characteristics for each converters is achieved minimizing the performance degradation from mismatch between channels.

A simple clock generator has been implemented to generate four phase timing clocks. Each clock is generated by routing one pulse out of four from the same original clock. By doing this, the timing skew between the clocks is minimized. Other techniques are also used to minimize the timing jitter of the clocks, such as distribution of the clocks using a tree structure that results in nearly equal propagation delay to all switches and latches in each of the four converters. Chip-On-Board testing architecture is adopted to test the chips. Chip-On-Board testing allows us to minimize the parasitic inductance due to bonding wires. Since the dies are directly bonded onto the Printed Circuit Board (PCB), the parasitic inductance due to

package leads are totally avoided. From the testing results, about 1 bit of performance improvement is achieved comparing with conventional testing where the dies are packaged and soldered to the PCB.

The four converter array together achieved a highest acquisition speed of 900MS/s. The measured SNDR is over 31dB at 900MHz with analog input at 1.1MHz, compared with SNDR of 28dB with analog input at 141kHz[8]. The SFDR of the ADC is higher than 30dB with analog input higher than 400MHz at sampling speed of 900MS/s. It achieves 5dB higher than reported [8]. The SNDR of the converter is higher than 29dB with input frequency up to 150MHz at sampling frequency of 600MS/s. The total active area is 2.08mm^2 with a power dissipation of 250mW at 600MS/s and 450mW at 900MS/s.

In the second part of this dissertation, a novel Voltage Controlled Resistor scheme has been described for mismatch adjustment in analog CMOS circuits. A macro-model of this device has also been proposed and demonstrated. The DC characteristics of the DC model have been confirmed using finite element device simulation software ATLAS^{TM} and experimentally verified using a conventional TSMC 0.25 μm CMOS process. From the simulation results, it shows that the current units can be calibrated to 0.01% precision. This trimming capability demonstrated high potentiality for mismatch adjustment in precision analog CMOS circuits, such as high resolution and high speed digital-to-analog converters which are based on equal current sources.

APPENDIX A TRANSIENT RESPONSE OF THE PREAMPLIFIER

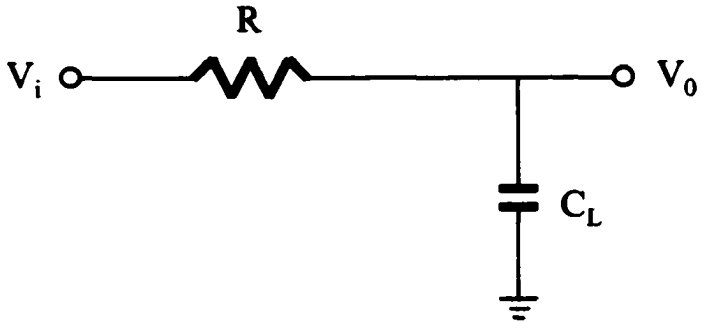


Figure A.1 Simplified model for a preamp

The preamplifier can be modeled as a simple low pass filter shown in Figure A.1. The transfer function for the model can be derived as

$$H(S)=\frac{V_0(S)}{V_i(S)}=\frac{1}{SCR+1} \qquad \text{(A.1)}$$

Starting at t=0, a sine wave is applied at the input

$$V_i(t)=A\sin(\omega_1 t)u(t) \qquad \text{(A.2)}$$

Then, we can obtain at the output

$$V_0(S)=\frac{\omega_0}{S+\omega_0}\cdot A\frac{\omega_1}{S^2+\omega_1^{\,2}} \qquad \text{(A.3)}$$

and

$$\omega_0 = \frac{1}{RC}$$

(A.3) can be rewritten as

$$V_0(S) = \frac{a}{S+\omega_0} + \frac{b}{S+j\omega_1} + \frac{c}{S-j\omega_1}$$
$$= \frac{(a+b+c)S^2 + (-jb\omega_1 + b\omega_0 + jc\omega_1 + c\omega_0)S + (a\omega_1^{\,2} - jb\omega_0\omega_1 + jc\omega_0\omega_1)}{(S+\omega_0)(S^2+\omega_1^{\,2})} \qquad \text{(A.4)}$$

Comparing (A.3) with (A.4), we have

$$\begin{aligned} &a+b+c=0 \\ &-jb\omega_1 + b\omega_0 + jc\omega_1 + c\omega_0 = 0 \\ &a\omega_1^{\,2} - jb\omega_0\omega_1 + jc\omega_0\omega_1 = \omega_0\omega_1 \end{aligned} \qquad \text{(A.5)}$$

Solve (A.5), we obtain

$$\begin{aligned} a &= \frac{\omega_0\omega_1}{\omega_1^{\,2}+\omega_0^{\,2}} \\ b &= \frac{-j\omega_0\omega_1 - \omega_0^{\,2}}{j2(\omega_1^{\,2}+\omega_0^{\,2})} \\ c &= \frac{\omega_0^{\,2} - j\omega_0\omega_1}{j2(\omega_1^{\,2}+\omega_0^{\,2})} \end{aligned} \qquad \text{(A.6)}$$

Substituting (A.6) into (A.4), we get

$$V_0(S) = \frac{-\dfrac{\omega_0\omega_1}{\omega_1^{\,2}+\omega_0^{\,2}}}{S+\omega_0} + \frac{\dfrac{-j\omega_0\omega_1 - \omega_0^{\,2}}{j2(\omega_1^{\,2}+\omega_0^{\,2})}}{S+j\omega_1} + \frac{\dfrac{\omega_0^{\,2} - j\omega_0\omega_1}{j2(\omega_0^{\,2}+\omega_1^{\,2})}}{S-j\omega_1} \qquad \text{(A.7)}$$

By doing inverse Laplace transform, we have

$$V_0(t) = \frac{\omega_0\omega_1}{\omega_1^2 + \omega_0^2} e^{-\omega_0 t} + \frac{-j\omega_0\omega_1 - \omega_0^2}{j2(\omega_1^2 + \omega_0^2)} e^{-j\omega_1 t} + \frac{\omega_0^2 - j\omega_1\omega_0}{j2(\omega_1^2 + \omega_0^2)} e^{j\omega_1 t} \quad \text{(A.8)}$$

(A.8) can be rewritten as

$$V_0(t) = \frac{\omega_0\omega_1}{\omega_1^2 + \omega_0^2} e^{-\omega_0 t} + \frac{\omega_0(\omega_0 \sin(\omega_1 t) - \omega_1 \cos(\omega_1 t))}{\omega_1^2 + \omega_0^2} \quad \text{(A.9)}$$

APPENDIX B VCR DC MODEL DERIVATION

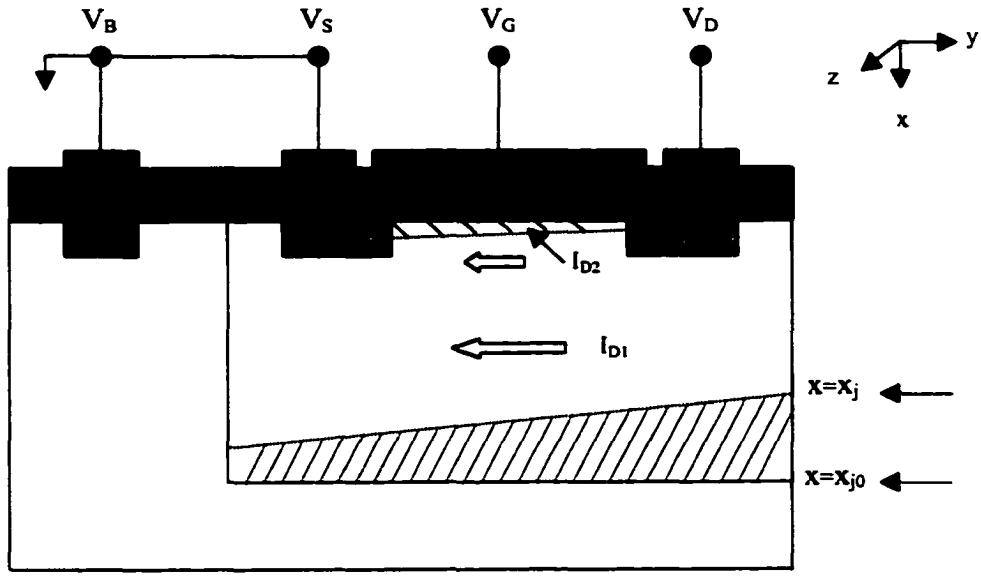


Figure B.1 Cross section of the VCR

The electron charge density at point (x,y) in the n-well is qn(x,y). Assume the electron mobility is $\mu(x)$, then we have

$$I_{D1} = \int_{Z=0}^{W_{eff}} \int_{x=0}^{x=x_j(y)} qu(x)n(x)\,dx\,dz\,\frac{dV(y)}{dy} \qquad \text{(B.1)}$$

Assuming the doping in n-well is constant, n(x) is equal to N_W. (N_W is the doping concentration in n-well)

$$I_{D1} = quN_W x_j(y)\frac{dV(y)}{dy}W_{eff} \qquad \text{(B.2)}$$

where W_{eff} is the effective width of n-well resistor.

$$x_j(y) = x_{j0} - \alpha\sqrt{\varphi + V(y) - V_B} \tag{B.3}$$

x_{j0} is the metallurgical junction depth. ϕ is the build-in voltage and α is the depletion width factor.

$$\varphi = \frac{kT}{q}\ln\left(\frac{N_w N_{sub}}{n_i^2}\right) \tag{B.4}$$

$$\alpha = \sqrt{\frac{2\varepsilon N_{sub}}{qN_w(N_w + N_{sub})}} \tag{B.5}$$

Combining equation (B.2),(B.3),(B.4) and (B.5), we have

$$I_{D1}dy = W_{eff}(q\mu N_w(x_{j0} - \alpha\sqrt{\varphi + V(y) - V_B})dV(y)) \tag{B.6}$$

Integrating both side of equation (6), we obtain

$$I_{D1}L_{eff} = W_{eff}(q\mu N_w x_{j0}V_{DS} - quN_w\alpha\frac{2}{3}(\varphi + V(y) - V_B)^{\frac{3}{2}}|_{V_S}^{V_D}) \tag{B.7}$$

Rearrange equation (A.7), we get

$$I_{D1} = W_{efff}\frac{q\mu N_W x_{j0}V_{DS} - \frac{2}{3}q\mu N_W\alpha[(\varphi + V_D - V_B)^{\frac{3}{2}} - (\varphi + V_S - V_B)^{\frac{3}{2}}]}{L_{eff}} \tag{B.8}$$

Assuming $V_S = V_B$, then

$$\begin{aligned}(\varphi + V_D - V_B)^{\frac{3}{2}} = (\varphi + V_{DB})^{\frac{3}{2}} &= V_{DB}^{\frac{3}{2}}(1 + \frac{\varphi}{V_{DS}})^{\frac{3}{2}} \\ &\approx V_{DB}^{\frac{3}{2}} + \frac{3}{2}\varphi V_{DB}^{\frac{1}{2}} + \frac{3}{4}\varphi V_{DB}^{-\frac{1}{2}} \\ &= V_{DS}^{\frac{3}{2}} + \frac{3}{2}\varphi V_{DS}^{\frac{1}{2}} + \frac{3}{4}\varphi V_{DS}^{-\frac{1}{2}}\end{aligned} \tag{B.9}$$

With equation (A.9), equation (A.8) can be simplified as

$$I_{D1} = \frac{q\mu N_W V_{DS} W_{eff}}{L_{eff}} x_{jeff} \qquad \text{(B.10)}$$

where

$$x_{jeff} = x_{j0} - \frac{2}{3}\alpha(V_{DS}^{\frac{1}{2}} + \frac{3}{2}\varphi V_{DS}^{-\frac{1}{2}} + \frac{3}{4}\varphi V_{DS}^{-\frac{3}{2}}) \qquad \text{(B.11)}$$

BIBLIOGRAPHY

[1] Stanley L. Hurst, *VLSI Custom Microelectrnoics*,Marcel Dekker, Inc., 1998

[2] Hemant Thapar, Sang-Soo Lee, et al. "Hard Disk Drive Read Channels: Technology and Trends", *Proceedings of the Custom Integrated Circuits*, pp. 309-316, 1999

[3] Sanroku Tsukamoto et al., "A CMOS 6-b, 200Msample/s, 3V-Supply A/D Converter for a PRML Read Channel LSI", *IEEE Journal of Solid-State Circuits*, Vol. 31, no. 11, pp. 1831-1836, Nov. 1996

[4] G. Tuttle et al., "A 16MB/s PRML read/write data channel", *ISSCC Digest of Technical Papers*, pp. 64-65, Feb. 1996

[5] J. Sonntag et al., "A high speed, low power PRML read channel device" *IEEE Transactions on Magnetics*, Vol. 31, no. 2, pp. 1186-1195, Mar. 1995

[6] R. Cideciyan et al., "A PRML system for digital magnetic recording", *IEEE Journal on Selected Areas in Communications*, Vol. 10, no. 1, pp. 38-56, 1992

[7] Sanroku Tsukamoto et al., "A CMOS 6-b, 200Msample/s, 3V-Supply A/D Converter for a PRML Read Channel LSI", *IEEE Journal of Solid-State Circuits*, Vol. 31, no. 11, pp. 1831-1836, Nov. 1996

[8] Uyttenhove, K., "A 6-bit 1GHz Acquisition Speed CMOS Flash ADC with Digital Error Correction", *IEEE Custom Integrated Circuits Conference*, pp. 249-252, 2000

[9] Sushihara, K., "A 6-b 800Msample/s CMOS A/D Converter", *IEEE International Solid-State Circuits Conference*, pp. 428-429, 2000

[10] Nagaraj, K., "A 700Msample/s 6b Read Channel A/D Converter with 7b Servo Mode", *IEEE International Solid-State Circuits Conference*, pp. 426-427, 2000

[11] Joe Spalding, Declan Dalton, "A 200Msamples/s 6b Flash ADC in 0.6um CMOS", *ISSCC Digest of Technical Papers*, pp. 320-321, Feb., 1996

[12] Iuri Mehr, Declan Dalton, "A 500MSample/s 6-Bit Nyquist Rate ADC for Disk Drive Read Channel Applications", *IEEE Journal of Solid State Circuits*, pp. 912-920, Vol. 34, July 1999

[13] P.Setty, J. Barner, etc., "A 5.75b 350Msample/s or 6.75b 150Msample/s Reconfigurable Flash ADC for a PRML Read Channel", *ISSCC Digest of Technical Papers*, pp. 148-149, Feb., 1998

[14] Yuko Tamba, Kazuo Yamakidd, "A CMOS 6b 500Msample/s ADC for a Hard Disk Drive Read Channel", *ISSCC Digest of Technical Papers*, pp. 324-325, Feb., 1999

[15] Xiao, P. et al., "A 4b 8Gsample/s A/D converter in SiGe bipolar technology", *ISSCC Digest of Technical papers*, pp. 124-125, Feb. 1997

[16]Ducourant, T., "3GHz, 150mW, 4 Bit GaAs Analog to Digital Converter", *Technical Digest – GaAs IC symposium*, pp. 209-212, 1992

[17] Ducourant, T., "A bit, 2.2Gs/s monolithic A/D converter with gigahertz bandwidth, and 6 bit A/D converter system", *Technical Digest – GaAs IC Symposium*, pp. 337-340, 1989

[18] Tsutomu Wakimoto et al., "Si Bipolar 2GS/s 6b Flash A/D Convertersion LSI", *ISSCC Digest of Technical Papers*, pp. 232-233, Feb., 1988

[19] Ken Poulton et al., "A 1-GHz 6-bit ADC System", *IEEE Journal of Solid-State Circuits*, Vol. SC-22, no., 6, Dec. 1987

[20] J. Van Valberg and R. J. van de Plassche, "An 8-bit 650MHz folding ADC", *IEEE Journal of Solid-State Circuits*, Vol. 27, pp.1662-1666, Dec. 1992

[21] Akira Matsuzawa et al., "An 8b 600MHz Flash A/D Converter with Multistage Duplex Gray Coding", *Symposium on VLSI Circuits, Digest of Technical Papers*, pp. 113-114, 1991

[22] Tuko Tamba, Kazuo Yamakido, "A CMOS 6b 500Msample/s ADC for a Hard Disk Drive Read Channel", *ISSCC, Digest of Technical Papers*, pp. 324-325, 1999

[23] Dingwall, A.G.F, "Monolithic expandable 6b 20MHz CMOS/SOS A/D converter", *IEEE Journal of Solid-State Circuits*, vol. SC-14, pp. 926-932, Dec., 1979

[24] William C. Black, Jr., David A. Hodges, "Time Interleaved Converter Arrays", *IEEE Journal of Solid State Circuits*, Vol. SC-15, no. 6, pp. 1022-1029, Dec. 1980

[25] Moonsik Song, "A 10-bit 80MHz 3.0V CMOS D/A Converter for Video Application", *IEEE Transactions on Consumer Electronics*, Vol. 43, No.3, pp. 868-872, August 1997

[26] Yasuhiro Yamada, "A 16-Bit CMOS D/A Converter for Digital Audio Applications", *IEEE Transactions on Consumer Electronics*, Vol. CE-33, No. 3, pp. 321-327, August 1987

[27] H.S. Lee, D.A. Hodges, and P.R. Gray, "A self-calibrating 15b CMOS A/D converter", *IEEE J.Solid-State Circuits*, Vol. SC-19, pp 813-819, Dec., 1984

[28] Rudy Van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer Academic Publishers, 1994

[29] D.Wouter J.Groeneveld, "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters", *IEEE J. Solid-State Circuits*, Vol. 24, No. 6, pp. 1517-1522, Dec. 1989

[30] David Johns, Ken Matin, *Analog Integrated Circuit Design*, John Wiley & Sons, Inc, 1997

[31] Doernberg, J., "Full-Speed Testing of A/D Converters", *IEEE Journal of Solid-State Circuits*, Vol. SC-19, No. 6, pp. 820-827, Dec., 1984

[32] Carlo Marandi and Luca Niccolai, "An Improved Code Density Test for the Dynamic Characterization of Flash A/D Converters", *IEEE Transactions on Instrumentation and Measurements*, Vol. 43, no. 3, pp. 384-388, June 1994

[33] Ginetti, B., Jespers, P., "Reliability of Code Density Test for High Resolution ADCs", *Electronics Letters*, Vol. 27, No. 24, pp. 2231-2233, Nov., 1991

[34] Mahmoud Fawzy Wagdy and Wai-Man NG, "Validity of Uniform Quantization Error Model for Sinusoidal Signals Without and With Dither", *IEEE Transactions on Instrumentation and Measurement*, Vol. 38, no. 3, pp. 718-722, June 1989

[35] James H. Atherton and H. Thomas Simmonds, "An Offset Reduction Technique for Use with CMOS Integrated Comparators and Amplifiers", *IEEE Journal of Solid-State Circuits*, Vol. 27, no. 8, pp. 1169-1175, August, 1992

[36] Yoshinobu Nakagome et al., "An Experimental 1.5-V 64-Mb DRAM", *IEEE Journal of Solid-State Circuits*, Vol. 26, no. 4, pp. 465-472, April, 1991

[37] Thomas Byunghak Cho and Paul R. Gray, "A 10b, 20Msample/s, 35mW Pipeline A/D Converter", *IEEE Journal of Solid-State Circuits*, Vol. 30, no. 3, pp. 166-172, March, 1995

[38] Tatsuji Matsuura et al., "An 8b 20MHz CMOS Half-Flash A/D Converter", *ISSCC, Digest of Technical Papers*, pp. 220-221Feb., 1988

[39] Mahmoud Fawzy Wagdy and Selim S. Awad, "Determining ADC Effective Number of Bits Via Histogram Testing", *IEEE Transactions on Instrumentation and Measurement*, Vol. 40, no. 4, pp. 770-772, August, 1991

[40] N. Fukushima et al., "A CMOS 40MHz 8b 105mW two-step ADC", *ISSCC, Digest of Technical Papers*, pp. 14-15, Feb, 1989

[41] S. Hosotani et al., "An 8-bit 20MS/s CMOS A/D converter with 50mW power consumption", *IEEE Journal of Solid-State Circuits*, Vol. 25, no. 1, pp. 167-172, Feb., 1990

[42] Keiko Makie-Fukuda et al., "Measurement of Digital Noise in Mixed-Signal Integrated Circuits", *IEEE Journal of Solid-State Circuits*, Vol. 30, no. 2, pp. 87-92, February, 1995

[43] Stephen Henry Lewis, *Video-Rate Analog-to-Digital Conversion using Pipelined Architecture*, Ph.D dissertation, pp. 82-88, 1987

[44] Bing J. Sheu, al., et. "Switch-Induced Error Voltage on a Switched Capacitor", *IEEE Journal of Solid State Circuits*, SC-19, No. 4, pp. 519-525, Aug., 1984

[45] P.J. Lim, *Performance Limits of Circuits for Analog-to-Digital Conversion*, Ph.D Dissertation, Standford University, Mar. 1991

[46] Abraham Peled and Bede Liu, *Digital Signal Processing, Theory, Design*, and Implementation, Johe Wiley & Sons, 1976

[47] William C. Black, Jr., *High Speed CMOS A/D Converter Techniques*, Ph.D Dissertation, University of Berkeley, Nov., 1980

[48] Jenq, Y. C., "Digital spectra of nonuniformly sampled signals: Fundamentals and high speed waveform digitizers", *IEEE Transactions on Instrumentation and measurement*, Vol. 39, No. 1, pp. 969-971, Feb., 1990

[49] Mangelsdorf, C. "A 400-MHz Input Flash Converter with Error Correction", *IEEE Journal of Solid State Circuits*, Vol. 25, No. 1, pp. 184-191, Feb., 1990

[50] Deevy, K. T., Quinlan, P., *ROM Encoder Circuit for Flash ADC's with Transistor Sizing to Prevent Sparkle Errors*, US Patent 5,644,312

[51] Weigandt, T. C., *Low-Phase-Noise, Low-Timing-Jitter Design Techniques for Delay Cell Based VCOs and Frequency Systhesizers*, Ph. D Dissertation, pp. 80-81, 1998

[52] Mark R. Kagey, *Modified Quasi-Gray Digital Encoding Technique*, U.S Patent, 4,975,698, Dec. 1990

[53] Kenneth T. Deevy, Philip Quinlan, *ROM Encoder Circuit for Flash ADC's with Transistor Sizing to Prevent Sparkle Errors*, U. S Patent, 5,644,312

[54] D.K.Su et. al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", *IEEE Journal of Solid State Circuits*, vol. 31, no. 3, pp 344-353, Apr., 1993

[55] Thaddeus Gabara, "Reduced Ground Bounce and Improved Latch-Up Suppression Through Substrate Conduction", *IEEE Journal of Solid State Circuits*, Vol.,23, No. 5, pp. 1224-1232, Oct., 1988

[56] Electrical Model Report from Amkor Technology, Report EM-98-69, September 18, 1998

[57] Howard Johnson and Martin Graham, *High –Speed Digital Design*, Prentice Hall PTR, 1993

[58] Mark Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*, IEEE Press, 1996

[59] Lin Wu , W. Black, "A Low-Jitter Skew-Calibrated Multi-Phase Clock Generator for Time-Interleaved Applications", ISSCC, 2001

[60] A.S Grove, *Physics and Technology of Semiconductor Devices*, John Wiley and Sons, Inc., 1967

[61] Richard V. H. Booth, Colin C. McAndrew, "A 3-Terminal Model for Diffused and Ion-Implanted Resistors", *IEEE Transactions on Electron Devices*, Vol. 44, NO. 5, pp. 809-814, May 1997

[62] James Victory, Colin C. McAndrew, Jeff Hall, and Mike Zunino, "A 4-Treminal Compact Model for High Voltage Diffused Resistors with Field Plates", *IEEE BCTM* 8.4, pp. 139-142

[63] Rolf Enderlein, Norman J. M. Horing, *Fundamentals of Semiconductor Physics and Devices*, World Scientific, 1997

[64] Patrick G. Drennan, "Diffused Resistor Mismatch Modeling and Chanracterization", *IEEE BCTM* 1.3, pp. 27-30

[65] D.Wouter J.Groeneveld, "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters", *IEEE Journal of Solid-State Circuits*, Vol. 24, No. 6, Dec. 1989

[66] Baiying Yu, et al "*Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*", pp. 563-566, 1998

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my major advisor, Prof. William C. Black, Jr. for his support and guidance through this research.

I would like to thank all my committee members, Prof. Chris Chong-Nuen Chu, Prof. Marwan Hassoun, Prof. Wolfgang Kliemann and Prof. Robert Weber for being in my committee. In particular, I thank Dr. Robert Weber for his help in high speed Printed Circuit Board design.

I thank our secretary Ms. Maria Blanco in maintaining nice environment in the Carver lab and her patience in ordering electronic parts.

I thank Mr. Jason Boyd and Mr. Larry Louis from Polarfab for their technical support.

I thank Dr. Xiaoliang Zhang for his spiritual and technical support and appreciate his help in all aspects.

I would like to express my thanks to all my colleagues for making my stay enjoyable.

This research was sponsored by Texas Instruments Inc. Testing was done in Carver Lab which supported by Texas Instruments, Rockwell Collins, Rocketchips and Roy J. Carver Charitable Trust. I appreciate all these contributions.